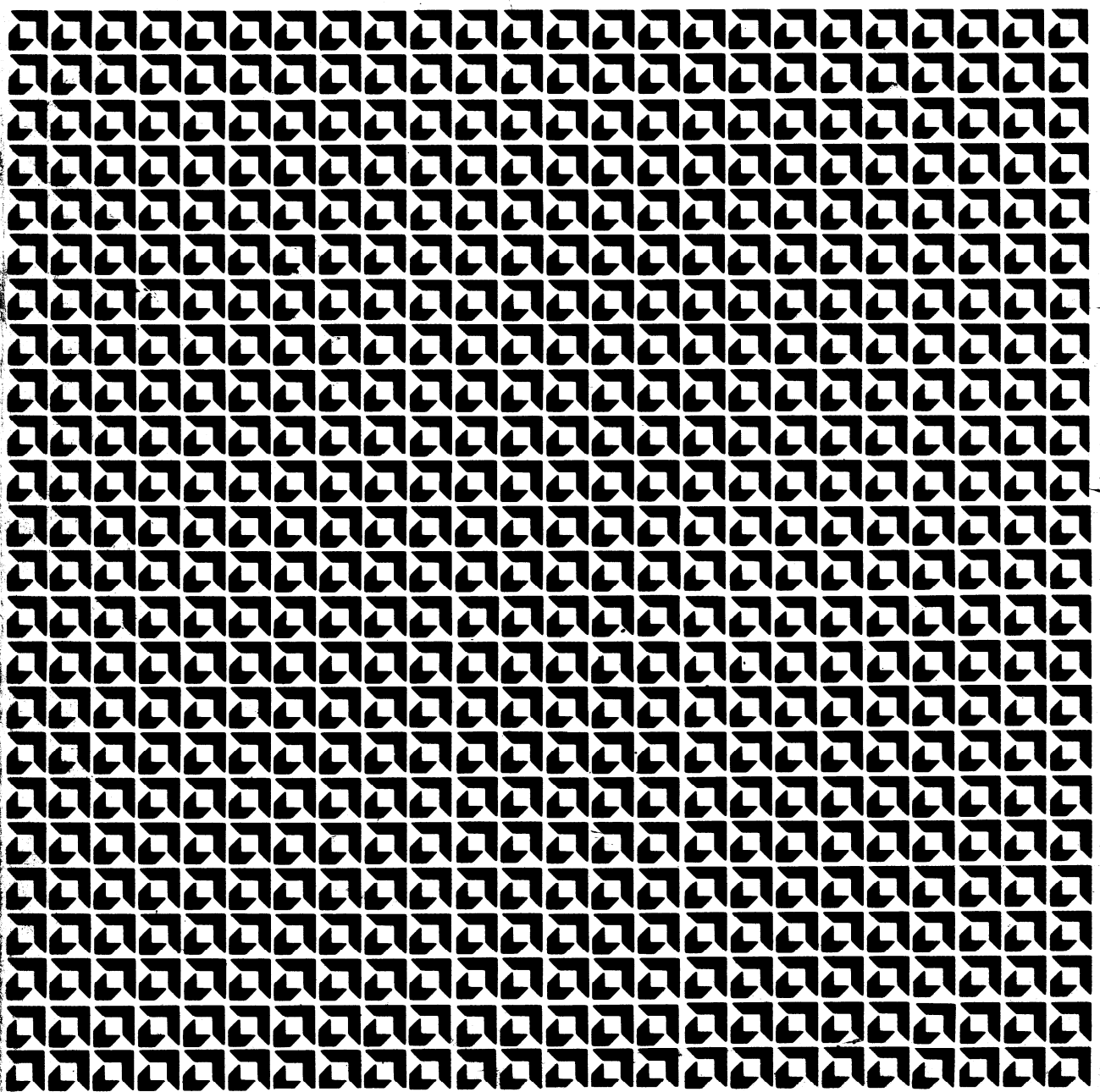


Schottky And Low-Power Schottky Bipolar Memory, Logic And Interface



Advanced Micro Devices

Schottky And Low-Power Schottky
Bipolar Memory, Logic And Interface

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FUNCTIONAL INDEX AND SELECTOR GUIDE

This guide divides the AMD Low Power Schottky and Schottky TTL Product Line by function into three basic performance categories:

1. High Performance Low-Power Schottky
Ex. 25LS174 Six Bit Register. $f_{max} = 40\text{MHz}$ (Min.)
2. Standard Low-Power Schottky
Ex. 74LS174 Six Bit Register. $f_{max} = 30\text{MHz}$ (Min.)
3. High-Speed Schottky
Ex. 74S174 Six Bit Register. $f_{max} = 75\text{MHz}$ (Min.)

DESCRIPTION	HIGH PERFORMANCE LOW-POWER SCHOTTKY		STANDARD LOW-POWER SCHOTTKY		HIGH-SPEED SCHOTTKY	
	DEVICE	PAGE	DEVICE	PAGE	DEVICE	PAGE
DECADE COUNTERS						
Synchronous BCD Decade Counter, Asynchronous Clear	25LS160	2-34	54/74LS160	3-22	54/74S160 93S10	4-84 4-120
Synchronous BCD Decade Counter, Synchronous Clear	25LS162	2-34	54/74LS162	3-22		
BINARY COUNTERS						
Synchronous Four-Bit Binary Counter, Asynchronous Clear	25LS161	2-34	54/74LS161	3-22	54/74S161 93S16	4-84 4-120
Synchronous Four-Bit Binary Counter, Synchronous Clear	25LS163	2-34	54/74LS163	3-22		
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Synchronous BCD Decade Up-Down Counter; Dual Clock	25LS192	6-6	54/74LS192	6-6		
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64-Bit RAM, Three-State					27S03 54/74S189	4-40 4-98
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32 x 8 Programmable ROM, Three-State	27LS09	2-66			27S09	4-46
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256 x 4 Programmable ROM, Three-State	27LS11	2-72			27S11	4-52
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Dual Four-Input Multiplexer	25LS153	2-26	54/74LS153	3-14	54/74S153	4-76
Three-State Dual Four-Input Multiplexer	25LS253	2-26	54/74LS253	3-14	54/74S253	4-76
Quad Two-Input Multiplexer; Non-Inverting	25LS157	2-30	54/74LS157	3-18	54/74S157 93S22	4-80 4-80
Three-State Quad Two-Input Multiplexer; Non-Inverting	25LS257	2-56	54/74LS257	3-44	54/74S257	4-106
Quad Two-Input Multiplexer; Inverting	25LS158	2-30	54/74LS158	3-18	54/74S158	4-80
Three-State Quad Two-Input Multiplexer; Inverting	25LS258	2-56	54/74LS258	3-44	54/74S258	4-106

Am27LS08 • Am27LS09

Low-Power Schottky 32-Word by 8-Bit PROMS

PRELIMINARY DATA

Distinctive Characteristics

- Highly reliable polysilicon fuses
- Pin compatible with types IM5600/5610, 82S23/123, MM5330/31, SN74188 and HPROM 8256
- Typical fusing time of 200 μ s/bit
- Three-state and open collector versions
- 50 ns maximum access time at 5.0V and 25°C

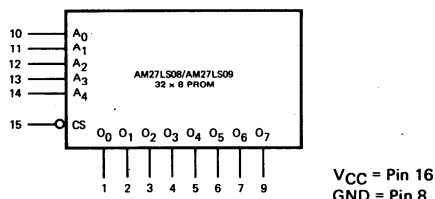
FUNCTIONAL DESCRIPTION

The Am27LS08 and Am27LS09 are electrically programmable Schottky TTL read only memories. Both devices are organized as 32 words of 8 bits each; the Am27LS08 has open collector outputs and the Am27LS09 has three-state outputs. The devices are shipped with all bits HIGH and each bit in the memory can be programmed to a LOW by applying appropriate voltages to the circuit. At each bit location on the circuit there is a narrow link of polysilicon material which is conductive, but which can be opened like a fuse by passing a short, high-current pulse through it. The fusing process simply melts the polysilicon at the center of the link and the two melted ends pull away from each other insuring a very reliable open circuit, which produces a LOW at the memory output.

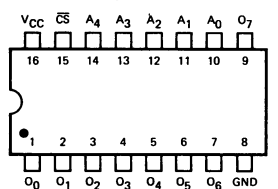
The programming voltage is applied at the output pin for the bit to be programmed, while the word to be programmed is selected by normal TTL levels on the address lines. The passage of current through the link is controlled by a programming pulse on the chip select input. There are two extra words and one additional bit for each word on the chip which are programmed at the factory during testing to insure high programming yields in devices shipped.

After programming, the device can be used for micro-program storage or random logic function generation, like any read-only memory. If the chip select input is held HIGH, the outputs will all turn off, so the outputs of several memories can be tied together for expansion.

LOGIC SYMBOL

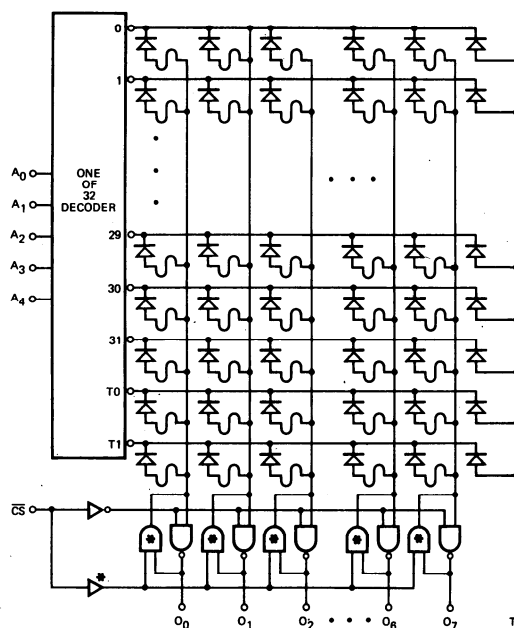


CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

BLOCK DIAGRAM



* = High Voltage Gate for Programming
T0 = Test Word
T1 = Test Word
TR = Test Rail

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27LS08DC
Hermetic DIP	-55°C to +125°C	AM27LS08DM
Flat Pack	-55°C to +125°C	AM27LS08FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27LS09DC
Hermetic DIP	-55°C to +125°C	AM27LS09DM
Flat Pack	-55°C to +125°C	AM27LS09FM

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	-0.5V to +7V
DC Voltage Applied to Outputs (Except During Programming)	-0.5V to +V _{CC} max.
DC Input Voltage (Address Inputs)	-0.5V to +5.5V
DC Voltage Applied to Outputs During Programming	25V
Output Current into Outputs During Programming	125 mA
DC Input Voltage (Chip Select Input)	-0.5V to +15.5V
DC Input Current	-30mA to +5mA

OPERATING RANGE

Am27LS08XC, Am27LS09XC	T _A = 0°C to +75°C	V _{CC} = 5.0V ±5%	COM'L
Am27LS08XM, Am27LS09XM	T _A = -55°C to +125°C	V _{CC} = 5.0V ±10%	MIL

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)**PRELIMINARY DATA**

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)		Max.	Units
V _{OH} (Am27S09 only)	Output HIGH Voltage	V _{CC} = MIN., I _{OH} = -2.0mA V _{IN} = V _{IH} or V _{IL}	2.4				Volts
V _{OL}	Output LOW Voltage	V _{CC} = MIN. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 8mA			0.4	Volts
			I _{OL} = 16mA			0.45	
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0				Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I _{IL}	Input LOW Current	V _{CC} = MAX., V _{IN} = 0.4V		-0.010		-0.100	mA
I _{IH}	Input HIGH Current	V _{CC} = MAX., V _{IN} = 2.7V				10	μA
I _I	Input HIGH current	V _{CC} = MAX., V _{IN} = 5.5V				1.0	mA
I _{SC} (Am27S09 only)	Output Short Circuit Current (Note 2)	V _{CC} = MAX., V _{OUT} = 0.0V	-12	-35		-85	mA
I _{CC}	Power Supply Current	All inputs = GND V _{CC} = MAX.			55	80	mA
V _I	Input Clamp Voltage	V _{CC} = MIN., I _{IN} = -18mA				-1.5	V
I _{CEX}	Output Leakage Current	V _{CC} = MAX V _{CS} = 2.4V	V _O = 4.5V			100	μA
			V _O = 2.4V			40	
			V _O = 0.4V			-40	

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE**PRELIMINARY DATA**

Parameter	Description	Test Conditions	Typ.		Max.		Units	
			5V 25°C	25°C	Com'l	Mil		
t _{AA}	Address Access Time	C _L = 30 pF R _L = 300Ω to V _{CC} and 600Ω to GND (16mA Load) Note 1	30	50	55	75	ns	
t _{EA}	Enable Access Time		Am27LS08	24	35	35	40	ns
			Am27LS09	30	40	40	50	
t _{ER}	Enable Recovery Time		18	35	35	40	ns	

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

PROGRAMMING THE Am27LS08 and Am27LS09

The Am27LS08 and Am27LS09 are shipped with a polysilicon fusible link at each bit location. The output of the memory with the link in place is HIGH. To program the device the fusible links are selectively opened; reading an open location produces a LOW at the memory output.

The link is opened by passing a large current through it from a voltage supply of 20 V on the memory output. The current is directed through the fuse by raising the chip select input to 15 volts. After a short programming pulse, the 20-volt supply is removed, the chip is enabled, and the output level is sensed to determine whether or not the link has opened. If it has not opened another programming sequence is initiated on the output and chip select lines. If the link has opened — that is, a LOW is sensed — the programming pulses are continued for 100 μ sec to insure that the bit has been programmed reliably.

Most links will open with a few one microsecond programming pulses. Occasionally a link will be a little stronger and will require longer programming pulse. The duration of the programming pulse may be gradually lengthened up to 8 μ sec until a total elapsed time of 100msec has been spent on one bit. A link which has not opened by 100ms is most likely defective, and further programming of the device should not be attempted.

The memories will become hot during the programming due to the large currents being passed. Programming pulses should not be applied to one device more than 1.6 seconds to avoid heat damage. If this programming time is ever exceeded, all power to the chip, including V_{CC} , should be removed for a period of 300ms, after which programming can continue in cycles of 200 ms programming and 300 ms power off.

ceeded, all power to the chip, including V_{CC} , should be removed for a period of 300ms, after which programming can continue in cycles of 200 ms programming and 300 ms power off.

TEST WORDS

The Am27LS08 and Am27LS09 have an extra ninth bit on each word and two extra words. These extra locations are used by Advanced Micro Devices for testing purposes. The ninth bit on each word is accessible only on the die, and cannot be examined on packaged units. The two test words can be accessed on packaged units by applying a special address condition. The two test words are intended for AMD use only and will already be programmed in parts shipped. However, users may wish to access these test words for their own testing.

There is also a special address condition which forces all memory outputs to the LOW state, allowing verification of output LOW characteristics prior to programming.

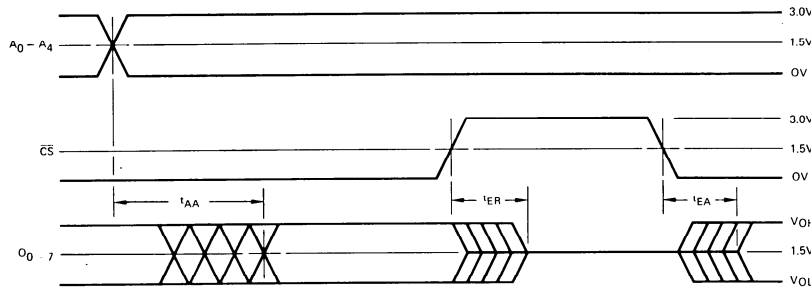
INPUTS (VOLTS)						OUTPUTS
\overline{CS}	A ₄	A ₃	A ₂	A ₁	A ₀	O ₇ - O ₀
0.4	X	13 \pm 1	13 \pm 1	0.4	X	Test word 0
0.4	X	13 \pm 1	13 \pm 1	2.4	X	Test word 1
0.4	X	13 \pm 1	X	X	X	All LOW

X = Don't Care (0 - 5V)

Note: 13V supply should be current limited with 300 ohm resistors.

Programming boards are available for the Data I/O automatic programmer. Order part no. 909-1119-1 for the two board set.

SWITCHING WAVEFORMS



Note: Level on output while \overline{CS} is HIGH is determined externally.

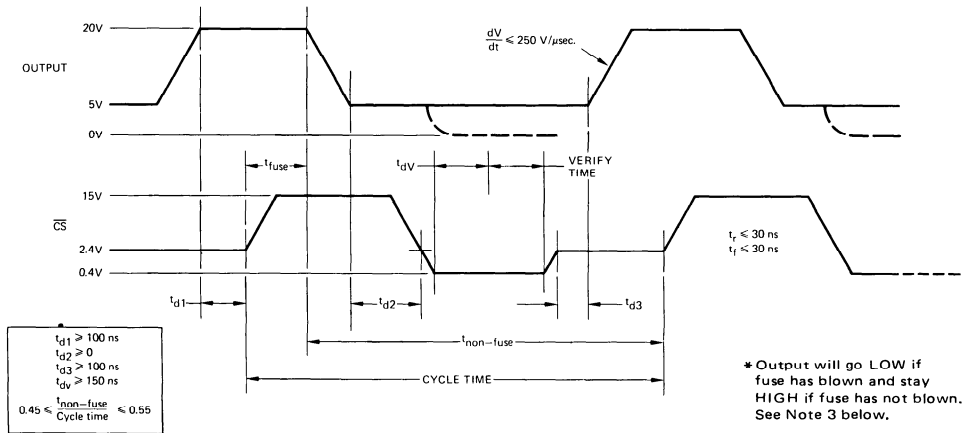
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

PROGRAMMING REQUIREMENTS

Parameter	Description	Min.	Max.	Units
V _{OP}	Voltage On Output to be Programmed	19.5	20.5	V
V _{ONP}	Voltage on Output not to be Programmed		V _{CC} +0.3	V
I _{ONP}	Current into Output not to be Programmed		20	mA
dv/dt	Rate of Voltage Change on Output		250	V/μs
V _{CSP}	Voltage on CS During Programming	14.5	15.5	V
V _{CSE}	Voltage on CS to Verify Chip		0.45	V
V _{CSD}	Voltage on CS to Disable Chip	2.4	5.5	V
V _{CCP}	V _{CC} During Programming	5.0	5.5	V
V _{ILP}	Address Input LOW Level		0.45	V
V _{IHP}	Address Input HIGH Level	2.4		V
t _{fuse}	Fusing Pulse Width	1.0	8.0	μs
t _{d1}	Delay Output = 20V to CS > 5.5V	100		ns
t _{d2}	Delay Output = 5V to CS ≤ 2.4V	0		ns
t _{dv}	Delay from CS ≤ 0.45 V to Verify	150		ns
t _{d3}	Delay CS ≥ 2.4V to Output > 5.5V	100		ns
Duty Cycle	Ratio of CS ≤ 5.5V to Total Period	45	55	%
t _{bit}	Elapsed Time Programming One Bit	0.1	100	ms
t _{cont}	Total Time Power Applied to Device During Programming		1.6	sec
t _{extra}	Time Programming Pulses are Applied After Blown Fuse is Detected	100		μs

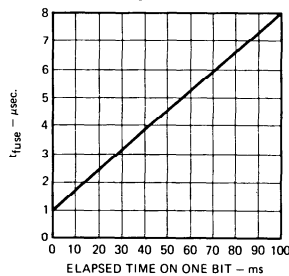
FUSING REQUIREMENTS



$t_{d1} \geq 100$ ns
 $t_{d2} \geq 0$
 $t_{d3} \geq 100$ ns
 $t_{dv} \geq 150$ ns
 $0.45 \leq t_{non-fuse} \leq 0.55$ Cycle time

- Notes:
1. Do not exceed 100ms accumulated programming time on one bit.
 2. After 1.6 seconds accumulated programming time, turn all power off for 300ms, then fuse for 200ms, then power off for 300ms, and so on.
 3. Continue fusing pulses for 100μs AFTER detecting open fuse.

Fuse Time Versus Time Attempting To Program One Bit



OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor. The program data may be submitted in the form of a truth table, but punched paper tapes are preferable since they can be handled automatically. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. Your distributor can also supply you with mark-sense cards on which pencil marks are used to indicate program data.

Paper tapes in the ASCII format below are usually the easiest way to specify the program. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

- 1) A leader of at least 25 rubouts.
- 2) The data patterns for all 32 words, starting with word 0, in the following format:
 - a) Any characters, including carriage return and line feed, except "B".
 - b) The letter "B", indicating the beginning of the data word.

- c) A sequence of eight Ps or Ns, starting with output 07.
 - d) The letter "F", indicating the finish of the data word.
 - e) Any text, including carriage return and line feed, except the letter "B".
- 3) A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
 An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

```

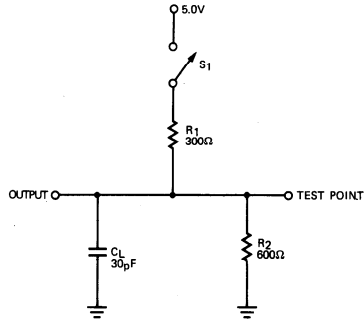
ϕϕϕ  BPNNPPNNPF  WORD ZERO (R) (L)
      BPPPPPPNNF  COMMENT FIELD (R) (L)
ϕϕ2  BNNNPPPPNF  ANY (R) (L)
      BNNNNNNNNF  TEXT (R) (L)
ϕϕ4  BPNNNNNNNF  CAN (R) (L)
      BNPPNPPNNF  GO (R) (L)
ϕϕ6  BPNNPPPPNF  HERE (R) (L)
      .....
ϕ31  BNNNPPPPNF  END (R) (L)
    
```

(R) = CARRIAGE RETURN
 (L) = LINE FEED

RESULTING DEVICE TRUTH TABLE (\overline{CS} = LOW)

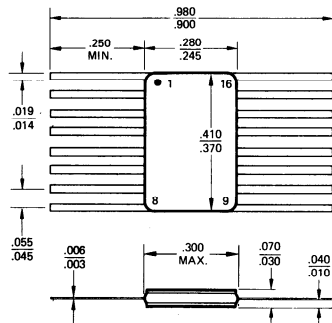
A ₄	A ₃	A ₂	A ₁	A ₀	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₀
L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	H	H	L	H	L	L	H	H	H	L	L
H	H	H	H	H	L	L	L	L	H	H	H	L

AC TEST CIRCUIT

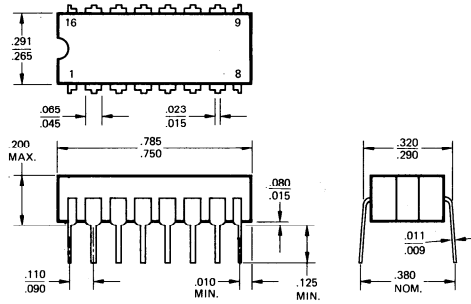


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