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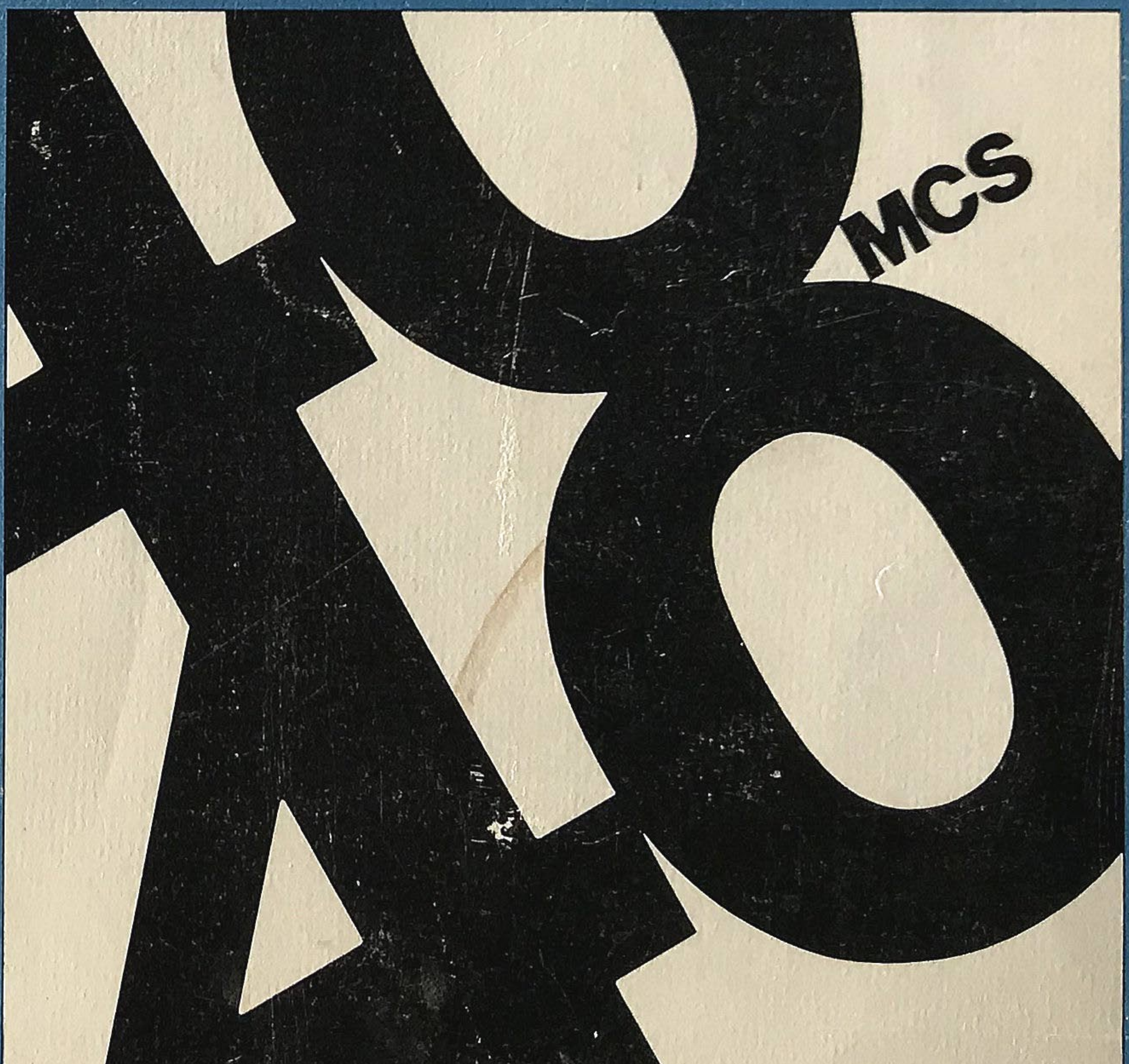
MCS-40™ Reference Card



98-101B

MCS-40™ Instruction Set

BASIC INSTRUCTIONS (* = 2 Word Instructions)

Hex Code	MNEMONIC	OPR D_3 D_2 D_1 D_0	OPA D_3 D_2 D_1 D_0	DESCRIPTION OF OPERATION
00	NOP	0 0 0 0	0 0 0 0	No operation.
1 - - -	*JCN	0 0 0 1 A_2 A_2 A_2 A_2	C_1 C_2 C_3 C_4 A_1 A_1 A_1 A_1	Jump to ROM address A_2 A_2 A_2 A_2, A_1 A_1 A_1 A_1 (within the same ROM that contains this JCN instruction) if condition C_1 C_2 C_3 C_4 is true, otherwise go to the next instruction in sequence.
2 - - -	*FIM	0 0 1 0 D_2 D_2 D_2 D_2	R R R 0 D_1 D_1 D_1 D_1	Fetch immediate (direct) from ROM Data D_2 D_2 D_2 D_2 D_1 D_1 D_1 D_1 to index register pair location RRR.
3 -	FIN	0 0 1 1	R R R 0	Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR.
3 -	JIN	0 0 1 1	R R R 1	Jump indirect. Send contents of register pair RRR out as an address at A_1 and A_2 time in the instruction cycle.
4 - - -	*JUN	0 1 0 0 A_2 A_2 A_2 A_2	A_3 A_3 A_3 A_3 A_1 A_1 A_1 A_1	Jump unconditional to ROM address A_3 A_3 A_3 A_3 A_2 A_2 A_2 A_2 A_1 A_1 A_1 A_1.
5 - - -	*JMS	0 1 0 1 A_2 A_2 A_2 A_2	A_3 A_3 A_3 A_3 A_1 A_1 A_1 A_1	Jump to subroutine ROM address A_3 A_3 A_3 A_3 A_2 A_2 A_2 A_2 A_1 A_1 A_1 A_1, save old address (up 1 level in stack.)
6 -	INC	0 1 1 0	R R R R	Increment contents of register RRRR.
7 - - -	*ISZ	0 1 1 1 A_2 A_2 A_2 A_2	R R R R A_1 A_1 A_1 A_1	Increment contents of register RRRR. Go to ROM address A_2 A_2 A_2 A_2 A_1 A_1 A_1 A_1 (within the same ROM that contains this ISZ instruction) if result ≠ 0, otherwise go to the next instruction in sequence.
8 -	ADD	1 0 0 0	R R R R	Add contents of register RRRR to accumulator with carry.
9 -	SUB	1 0 0 1	R R R R	Subtract contents of register RRRR to accumulator with borrow.
A -	LD	1 0 1 0	R R R R	Load contents of register RRRR to accumulator.
B -	XCH	1 0 1 1	R R R R	Exchange contents of index register RRRR and accumulator.
C -	BBL	1 1 0 0	D D D D	Branch back (down 1 level in stack) and load data DDDD to accumulator.
D -	LDM	1 1 0 1	D D D D	Load data DDDD to accumulator.
F0	CLB	1 1 1 1	0 0 0 0	Clear both. (Accumulator and carry)
F1	CLC	1 1 1 1	0 0 0 1	Clear carry.
F2	IAC	1 1 1 1	0 0 1 0	Increment accumulator.
F3	CMC	1 1 1 1	0 0 1 1	Complement carry.
F4	CMA	1 1 1 1	0 1 0 0	Complement accumulator.
F5	RAL	1 1 1 1	0 1 0 1	Rotate left. (Accumulator and carry)
F6	RAR	1 1 1 1	0 1 1 0	Rotate right. (Accumulator and carry)
F7	TCC	1 1 1 1	0 1 1 1	Transmit carry to accumulator and clear carry.
F8	DAC	1 1 1 1	1 0 0 0	Decrement accumulator.
F9	TCS	1 1 1 1	1 0 0 1	Transfer carry subtract and clear carry.
FA	STC	1 1 1 1	1 0 1 0	Set carry.
FB	DAA	1 1 1 1	1 0 1 1	Decimal adjust accumulator.
FC	KBP	1 1 1 1	1 1 0 0	Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
FD	DCL	1 1 1 1	1 1 0 1	Designate command line.

4040 ONLY INSTRUCTIONS

Hex Code	MNEMONIC	OPR D_3 D_2 D_1 D_0	OPA D_3 D_2 D_1 D_0	DESCRIPTION OF OPERATION
01	HLT	0 0 0 0	0 0 0 1	Executes Halt until interrupt received.
02	BBS	0 0 0 0	0 0 1 0	Return from subroutine and restore SRC.
03	LCR	0 0 0 0	0 0 1 1	Data RAM and ROM bank status loaded into ACC.
04	OR4	0 0 0 0	0 1 0 0	OR accumulator with IR4.

4040 ONLY INSTRUCTIONS (Continued)

Hex Code	MNEMONIC	OPR D_3 D_2 D_1 D_0	OPA D_3 D_2 D_1 D_0	DESCRIPTION OF OPERATION
05	OR5	0 0 0 0	0 1 0 1	OR accumulator with IR5.
06	AN6	0 0 0 0	0 1 1 0	AND accumulator with IR6.
07	AN7	0 0 0 0	0 1 1 1	AND accumulator with IR7.
08	DB0	0 0 0 0	1 0 0 0	Select ROM bank 0.
09	DB1	0 0 0 0	1 0 0 1	Select ROM bank 1.
0A	SB0	0 0 0 0	1 0 1 0	Select IR bank 0.
0B	SB1	0 0 0 0	1 0 1 1	Select IR bank 1.
0C	EIN	0 0 0 0	1 1 0 0	Enable interrupt detection.
0D	DIN	0 0 0 0	1 1 0 1	Disable interrupt detection.
0E	RPM	0 0 0 0	1 1 1 0	Load accumulator from 4289-controlled program RAM.

4001/4002/4008/4009/4289 INPUT/OUTPUT AND RAM INSTRUCTIONS (Refer to SRC Addressing)

Hex Code	MNEMONIC	OPR D_3 D_2 D_1 D_0	OPA D_3 D_2 D_1 D_0	DESCRIPTION OF OPERATION
2 -	SRC	0 0 1 0	R R R 1	Send register control. Send the address (contents of index register pair RRR) to ROM and RAM at X_2 and X_3 time in the instruction cycle.
E0	WRM	1 1 1 0	0 0 0 0	Write the contents of the accumulator into the previously selected RAM main memory character.
E1	WMP	1 1 1 0	0 0 0 1	Write the contents of the accumulator into the previously selected RAM output port. (Output Lines)
E2	WRR	1 1 1 0	0 0 1 0	Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)
E3	WPM	1 1 1 0	0 0 1 1	Write the contents of the accumulator into the previously selected half byte of read/write program memory (used with 4008/4009 or 4289 only)
E4	WR0	1 1 1 0	0 1 0 0	Write the contents of the accumulator into the previously selected RAM status character 0.
E5	WR1	1 1 1 0	0 1 0 1	Write the contents of the accumulator into the previously selected RAM status character 1.
E6	WR2	1 1 1 0	0 1 1 0	Write the contents of the accumulator into the previously selected RAM status character 2.
E7	WR3	1 1 1 0	0 1 1 1	Write the contents of the accumulator into the previously selected RAM status character 3.
E8	SBM	1 1 1 0	1 0 0 0	Subtract the previously selected RAM main memory character from accumulator with borrow.
E9	RDM	1 1 1 0	1 0 0 1	Read the previously selected RAM main memory character into the accumulator.
EA	RDR	1 1 1 0	1 0 1 0	Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)
EB	ADM	1 1 1 0	1 0 1 1	Add the previously selected RAM main memory character to accumulator with carry.
EC	RD0	1 1 1 0	1 1 0 0	Read the previously selected RAM status character 0 into accumulator.
ED	RD1	1 1 1 0	1 1 0 1	Read the previously selected RAM status character 1 into accumulator.
EE	RD2	1 1 1 0	1 1 1 0	Read the previously selected RAM status character 2 into accumulator.
EF	RD3	1 1 1 0	1 1 1 1	Read the previously selected RAM status character 3 into accumulator.

4269 Input/Output Instructions

Hex Code	MNEMONIC	OPR D_3 D_2 D_1 D_0	OPA D_3 D_2 D_1 D_0	DESCRIPTION OF OPERATION
E4	WRO	1 1 1 0	0 1 0 0	Set the input mode and output mode of the 4269 according to the value contained in the accumulator as follows: D_3 D_2 — 00 Individual, Scanned Displays, 8 or 16 Characters; 01 Gas Discharge, 20 Characters; 10 Gas Discharge, 18 Characters; 11 Gas Discharge, 16 Characters D_1 D_0 — 00 Sensor, Scanned; 01 Contact Keyboard, Scanned; 10 Encoded Keyboard, not Scanned; 11 Not Used
2-	SRC	0 0 1 0	R R R 1	The contents of the register pair RRR are used to select the 4269 (1st two bits of first register will contain 01, the binary address of a 4269). After a WRO instruction has set the mode of the 4269, an SRC preceding additional I/O instructions is interpreted as follows, depending on the mode set: RRR_{even} $D_3D_2D_1D_0$ — RRR_{odd} $D_3D_2D_1D_0$ **For gas discharge mode:** 0100 $n_3n_2n_1n_0$ — Selects the nth display register 0110 $n_3n_2n_1n_0$ — Selects the nth display register and blanks the display (with binary 32) **For individual, scanned display mode:** 0100 $n_3n_2n_1n_0$ — Selects one of 16 display registers of Register A 0101 $n_3n_2n_1n_0$ — Selects one of 16 display registers of Register B 0110 $n_3n_2n_1n_0$ — Selects one of 16 display registers of Register A, with Register A outputs being placed at V_{ss} level (allowing the port to be blanked while allowing normal reading and writing) 0111 $n_3n_2n_1n_0$ — Selects one of 16 display registers of Register B, with Register B outputs being placed at V_{ss} level (allowing the port to be blanked while allowing normal reading and writing) **For scanned sensor mode:** 0100 $n_3n_2n_1x$ — n_3-n_1 indicates a sensor group to be read **For scanned keyboard or non-scanned encoded keyboard:** 01XX XXXX — SRC used only to select 4269
E7	WR3	1 1 1 0	0 1 1 1	Clears the keyboard/sensor and display logic and fills the display RAM with all blanks. (Does not change mode).

4269 Input/Output Instructions (Continued)

Hex Code	MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
For gas discharge display mode:				
E5	WR1	1 1 1 0	0 1 0 1	Resets the internal display register pointer to 0 and forces display memory to blank state.
For individual, scanned display mode:				
E5	WR1	1 1 1 0	0 1 0 1	Resets the internal display register pointer to 0 and forces display memory to blank state. Upper two bits of ACC select length of display as follows: D_3 0 Display B is 16 nibbles deep 1 Display B is 8 nibbles deep D_2 0 Display A is 16 nibbles deep 1 Display A is 8 nibbles deep
For individual, scanned display mode and gas discharge display mode:				
E0	WRM	1 1 1 0	0 0 0 0	Loads the contents of the register addressed by the internal display register pointer with the contents of ACC; then advances the displayed data by one digit in relation to the scan line timing, and increments the display register pointer. In the gas discharge mode, the display register pointer alternates between the A and B registers.[1]
E9	RDM	1 1 1 0	1 0 0 1	Loads ACC with the contents of the register addressed by the display register pointer and then increments the display register pointer. In the gas discharge mode, the display register pointer alternates between the A and B registers.[1]
E1	WMP	1 1 1 0	0 0 0 1	Loads the contents of the register addressed by the display register pointer with the contents of ACC.
EF	RD3	1 1 1 0	1 1 1 1	Loads ACC with the contents of the display register pointed to by the display register pointer.
For keyboard input modes:				
E6	WR2	1 1 1 0	0 1 1 0	Clears FIFO/RAM logic, the status buffer, and the INT line.
ED	RD1	1 1 1 0	1 1 0 1	Reads the first nibble of the current FIFO register position.
EE	RD2	1 1 1 0	1 1 1 0	Reads the second nibble of the current FIFO register position. FIFO register position is incremented to the next position.
EC	RDO	1 1 1 0	1 1 0 0	Loads ACC with the FIFO status.
For scanned sensor mode:				
E6	WR2	1 1 1 0	0 1 1 0	Clears the FIFO/RAM logic and the INT line.
ED	RD1	1 1 1 0	1 1 0 1	Loads into ACC the upper 4 bits of the 8-bit sensor RAM group previously addressed by an SRC instruction.
EE	RD2	1 1 1 0	1 1 1 0	Loads into ACC the lower 4 bits of the 8-bit sensor RAM group previously addressed by an SRC instruction.

Note 1: Alternation pattern is A_0, B_0, A_1, B_1, A_2, etc.

SRC Addressing for 4001, 4002, 4008, 4009, 4289

1.) DATA RAM CHARACTER

CHIP	REG.	CHAR.

CHIP—1 of 4 Data RAM chips
REG—1 of 4 registers in Data Chip
CHAR—1 of 16 4-bit characters in register

2.) DATA RAM STATUS CHARACTER

CHIP	REG.	N/A

CHIP—1 of 4 Data RAM chips
REG—1 of 4 registers in Data RAM chip
N/A—Bits are not revelant for this reference

3.) RAM OUTPUT PORT

PORT	N/A

PORT—The output port of 1 of 4 Data RAM chips within a Data RAM bank
N/A—Bits not relevant for this reference

4.) ROM INPUT OR OUTPUT PORT

PORTS	N/A

PORTS—1 of 16 ROM ports

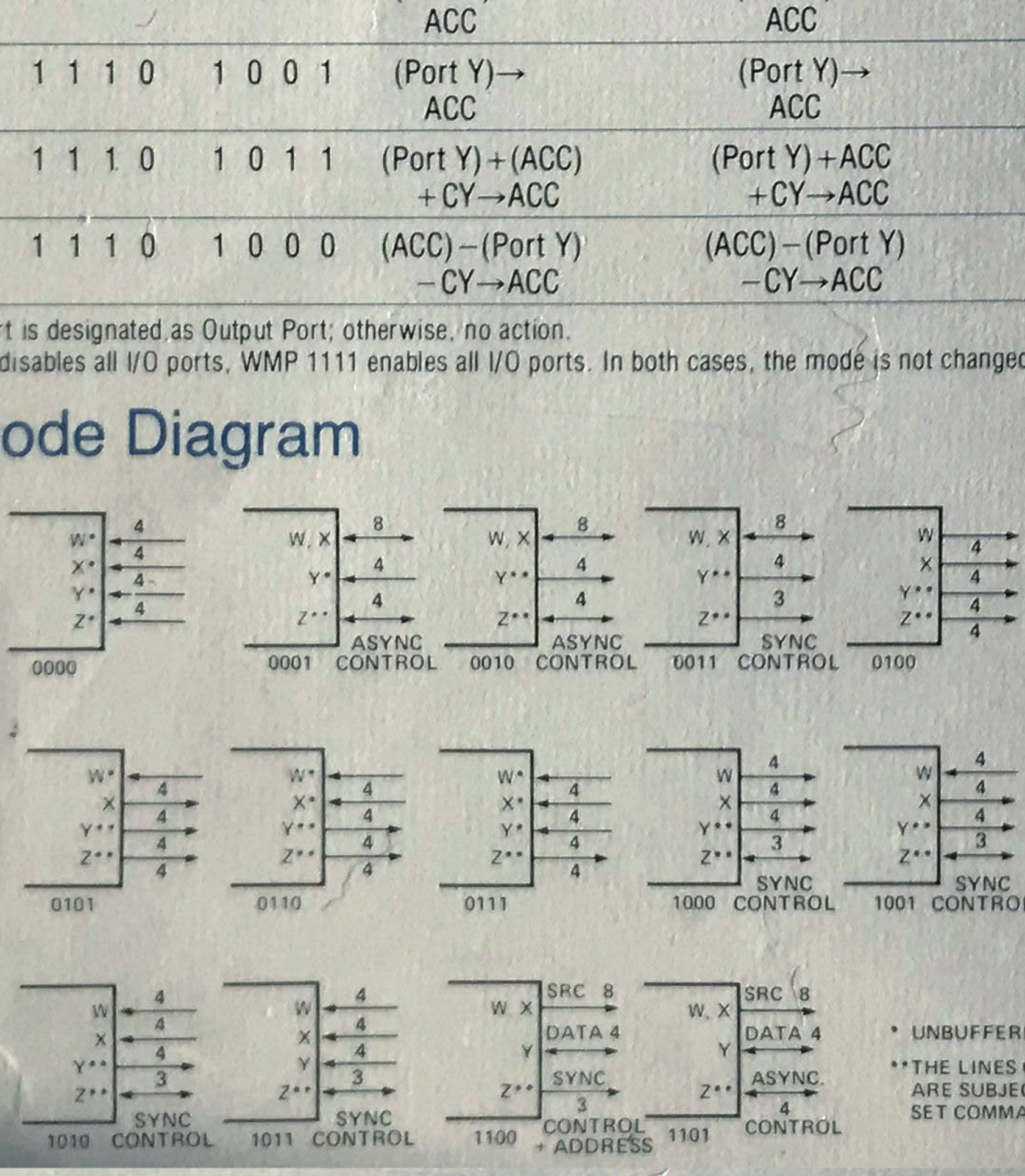
N/A—Bits not relevant for this reference

4265 Input/Output Instructions

Hex Code	MNEMONIC	OPR D_3 D_2 D_1 D_0	OPA D_3 D_2 D_1 D_0	DESCRIPTION OF OPERATION		
				Mode Independent Operations		
E0	WRM	1 1 1 0	0 0 0 0	The port Y or port Z bit designated by D_3 D_2 D_1 of the accumulator is set or reset according to D_0 (1=set, 0=reset).[1]		
E1	WMP	1 1 1 0	0 0 0 1	Sets the mode of the 4265 to the value contained in the accumulator.[2]		
				Mode Dependent Operations		
				Mode 1-3	**Mode 0, 4-11**	**Mode 12 and 13**
2-	SRC	0 0 1 0	R R R 1	For modes 0-11, the contents of register pair RRR are used to select the 4265 chip (first two bits of first register will contain 10 or 11, depending on chip address)		(RRR_{even})→ Port W (RRR_{odd})→ Port X
E4	WR0	1 1 1 0	0 1 0 0	(ACC)→ Port W	(ACC)→ Port W[1]	(ACC)→ Port Y
E5	WR1	1 1 1 0	0 1 0 1	(ACC)→ Port X	(ACC)→ Port X[1]	(ACC)→ Port Y
E6	WR2	1 1 1 0	0 1 1 0	(ACC)→ Port Y[1]	(ACC)→ Port Y[1]	(ACC)→ Port Y
E7	WR3	1 1 1 0	0 1 1 1	—	(ACC)→ Port Z[1]	(ACC)→ Port Y
EC	RD0	1 1 1 0	1 1 0 0	(Port W)→ ACC	(Port W)→ ACC	(Port Y)→ ACC
ED	RD1	1 1 1 0	1 1 0 1	(Port X)→ ACC	(Port X)→ ACC	(Port Y)→ ACC
EE	RD2	1 1 1 0	1 1 1 0	(Port Y)→ ACC	(Port Y)→ ACC	(Port Y)→ ACC
EF	RD3	1 1 1 0	1 1 1 1	(Port Z)→ ACC	(Port Z)→ ACC	(Port Y)→ ACC
E9	RDM	1 1 1 0	1 0 0 1	(Port Y)→ ACC	(Port Y)→ ACC	(Port Y)→ ACC
EB	ADM	1 1 1 0	1 0 1 1	(Port Y)+(ACC) +CY→ACC	(Port Y)+ACC +CY→ACC	(Port Y)+ACC +CY→ACC
E8	SBM	1 1 1 0	1 0 0 0	(ACC)−(Port Y) −CY→ACC	(ACC)−(Port Y) −CY→ACC	(ACC)−(Port Y) −CY→ACC

Note 1: Action if Port is designated as Output Port; otherwise, no action.
Note 2: WMP 1110 disables all I/O ports, WMP 1111 enables all I/O ports. In both cases, the mode is not changed.

4265 Mode Diagram



JCN Condition Codes

Special Mnemonic	C_1 C_2 C_3 C_4	Description
	0 0 0 0	Never Jump
JNT	0 0 0 1	Jump if Test = 0
JC	0 0 1 0	Jump if Carry = 1
	0 0 1 1	Jump if Test = 0 or Carry = 1
JZ	0 1 0 0	Jump if ACC = 0
	0 1 0 1	Jump if ACC = 0 or Test = 0
	0 1 1 0	Jump if ACC = 0 or Carry = 1
	0 1 1 1	Jump if ACC = 0 or Carry = 1 or Test = 0
	1 0 0 0	Jump Unconditionally
JT	1 0 0 1	Jump if Test = 1
JNC	1 0 1 0	Jump if Carry = 0
	1 0 1 1	Jump if Test = 1 and Carry = 0
JNZ	1 1 0 0	Jump if ACC ≠ 0
	1 1 0 1	Jump if ACC ≠ 0 and Test = 1
	1 1 1 0	Jump if ACC ≠ 0 and Carry = 0
	1 1 1 1	Jump if ACC ≠ 0 and Carry = 0 and Test = 1

System Monitor Commands

Command Format	Description
B Low Add., High Add.	Output content of program RAM from low add. to high add. to the TTY printer punch.
D Low Add., High Add.	Program RAM from low add. to high add. is displayed on TTY in Hex form.
E	Causes termination record and 60 null characters to be punched, creating an End-of-File mark.
I Low Add., High Add.	Complements each byte of program RAM from low add. to high add.
J	Causes monitor to use High Speed Reader for subsequent L or R commands.
K	Causes monitor to use TTY reader for subsequent L or R commands.
L Low Add., High Add.	Loads complemented BNPF paper tape into memory from low add. to high add.
M Low Add., High Add. Dest. Add.	Causes block of memory from low add. through high add. to be moved to location of memory starting at dest. add.
N	Causes 60 null characters to be printed. If TTY punch is on, will produce 6 in. of blank tape.
P Low Add., High Add. PROM Add.	Program RAM data from low add. thru high add. is transferred to 1602A or 1702A PROM beginning at PROM address.
R	Loads Hex format and paper tape into program RAM.
S Hex Add. (CR)	Used to display and/or modify the contents of individual program RAM locations
T Hex Add.	Transfers the contents of PROM to program RAM beginning at address specified for 256 bytes.
W Low Add., High Add.	Outputs program RAM low add. through high add. in Hex format to TTY printer/punch.

Notes: All addresses must be specified with no more than three Hex digits, otherwise monitor accepts only last three digits.
For special information on use and error conditions, refer to Intellec® 4/MOD40 Operators Manual, Section 4.0

Text Editor Commands

Command	Description
C	Copies one line from reader to tape punch.
nC	Copies "n" lines from reader to tape punch.
$C	Copies remaining lines to tape punch until a NULL character is sensed.
S	Skips one line of source tape.
nS	Skips "n" lines of source tape.
$S	Skips remaining lines of source tape until NULL is sensed.
A	Causes subsequent lines typed on Teletype to be copied on tape punch—Terminate with control-D.
:	Causes 60 NULL characters to be punched as trailer—Ends editing phase.

Assembler Pseudo-OPS

FORMAT			
Label	**Code**	**Operand**	**Description**
Opt.	ORG	"adr."	Next instruction or byte is assembled at address, "adr", "adr+1".
Req.	EQU	"exp"	The required LABEL is assigned value of "exp".
Req.	SET	"exp"	Same as EQU except required LABEL may be defined more than once.
*Opt.	IF	"exp"	Assembler evaluates "exp". If "exp" evaluates to zero, then statements between IF,
	ENDIF		ENDIF ignored, otherwise assemble.
*Req.	MACRO	"list"	Statements between MACRO and ENDM defined by MACRO LABEL -
	ENDM		
*Opt.	TITLE	"string"	Specified "string" will appear at top of each page of listing.
Opt.	BANK		Used for assembling for 4040 system with two ROM banks.
	END		Signifies the physical END of the program to assembler.

*Used with MAC4™ Cross Assembler only.

Assembler Error Messages

Code	Description
A	**A**ddress error caused by JUN or JMS referencing address not in range of 0 to 4095.
B	**B**alance error caused by parentheses in expression or quotes in ASCII string being unbalanced.
E	**E**xpression error caused by missing operator, comma, or misspelled op code.
F	**F**ormat error caused by missing or extraneous operand.
I	**I**llegal error caused by invalid ASCII character or numeric character exceeds base of number.
M	**M**ultiple definition occurs when symbol or Macro is defined more than once.
N	**N**esting error caused by IF or ENDIF improperly nested.
P	**P**hase error indicates element value changed between pass 1 and pass 2 of assembly.
Q	**Q**uestionable Syntax error caused by omitting operator.
R	**R**egister error indicates register specified is invalid.
S	**S**tack overflow indicates assembler's internal expression evaluation stack overflowed memory available.
T	**T**able overflow indicates assemblers symbol table space was exhausted.
U	**U**ndefined identifier indicates symbol in operand field was not previously defined.
V	**V**alue error caused by operand or expression value exceeds range required.
X	4040 only instruction—cannot be executed by 4004.
*?	Paper Tape Reader did not supply expected input.

Resident Assembler Commands

Command	Description
B or 1	Begins Pass 1 of assembly.
L or 2	Lists the program as Pass 2 of assembly.
P or 3	Punch object tape as Pass 3 of assembly.
J	Allows High Speed Reader to be used as source input.
K	Allows Teletype reader for source input (TTY reader is assumed as initial condition).
E	Used to invoke Text Editor for source tape editing.
X	Allows "X" error flag on listing for 4040 only instruction.

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