Intel 8008 instruction set

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	*HLT 1 8 - - - -	*HLT 1 8 - - - -	RLC 1 10 - - - C	RFC 1 10/6 - - - -	ADI d8 2 16 S Z P -	RST 0 1 10 - - - -	LAI d8 2 16 - - - -	RET 1 10 - - - -	INB 1 10 S Z P -	DCB 1 10 S Z P -	RRC 1 10 - - - C	RFZ 1 10/6 - - - -	ACI d8 2 16 S Z P -	RST 1 1 10 - - - -	LBI d8 2 16 - - - -	*RET 1 10 - - - -
1x	INC 1 10 S Z P -	DCC 1 10 S Z P -	RAL 1 10 - - - C	RFS 1 10/6 - - - -	SUI d8 2 16 S Z P -	RST 2 1 10 - - - -	LCI d8 2 16 - - - -	*RET 1 10 - - - -	IND 1 10 S Z P -	DCD 1 10 S Z P -	RAR 1 10 - - - C	RFP 1 10/6 - - - -	SBI d8 2 16 S Z P -	RST 3 1 10 - - - -	LDI d8 2 16 - - - -	*RET 1 10 - - - -
2x	INE 1 10 S Z P -	DCE 1 10 S Z P -		RTC 1 10/6 - - - -	NDI d8 2 16 S Z P -	RST 4 1 10 - - - -	LEI d8 2 16 - - - -	*RET 1 10 - - - -	INH 1 10 S Z P -	DCH 1 10 S Z P -		RTZ 1 10/6 - - - -	XRI d8 2 16 S Z P -	RST 5 1 10 - - - -	LHI d8 2 16 - - - -	*RET 1 10 - - - -
3x	INL 1 10 S Z P -	DCL 1 10 S Z P -		RTS 1 10/6 - - - -	ORI d8 2 16 S Z P -	RST 6 1 10 - - - -	LLI d8 2 16 - - - -	*RET 1 10 - - - -				RTP 1 10/6 - - - -	CPI d8 2 16 S Z P -	RST 7 1 10 - - - -	LMI d8 2 18 - - - -	*RET 1 10 - - - -
4x	JFC a16 3 22/18 - - - -	INP 0 1 16 - - - -	CFC a16 3 22/18 - - - -	INP 1 1 16 - - - -	JMP a16 3 22 - - - -	INP 2 1 16 - - - -	CAL a16 3 22 - - - -	INP 3 1 16 - - - -	JFZ a16 3 22/18 - - - -	INP 4 1 16 - - - -	CFZ a16 3 22/18 - - - -	INP 5 1 16 - - - -	*JMP a16 3 22 - - - -	INP 6 1 16 - - - -	*CAL a16 3 22 - - - -	INP 7 1 16 - - - -
5x	JFS a16 3 22/18 - - - -	OUT 8 1 12 - - - -	CFS a16 3 22/18 - - - -	OUT 9 1 12 - - - -	*JMP a16 3 22 - - - -	OUT 10 1 12 - - - -	*CAL a16 3 22 - - - -	OUT 11 1 12 - - - -	JFP a16 3 22/18 - - - -	OUT 12 1 12 - - - -	CFP a16 3 22/18 - - - -	OUT 13 1 12 - - - -	*JMP a16 3 22 - - - -	OUT 14 1 12 - - - -	*CAL a16 3 22 - - - -	OUT 15 1 12 - - - -
6x	JTC a16 3 22/18 - - - -	OUT 16 1 12 - - - -	CTC a16 3 22/18 - - - -	OUT 17 1 12 - - - -	*JMP a16 3 22 - - - -	OUT 18 1 12 - - - -	*CAL a16 3 22 - - - -	OUT 19 1 12 - - - -	JTZ a16 3 22/18 - - - -	OUT 20 1 12 - - - -	CTZ a16 3 22/18 - - - -	OUT 21 1 12 - - - -	*JMP a16 3 22 - - - -	OUT 22 1 12 - - - -	*CAL a16 3 22 - - - -	OUT 23 1 12 - - - -
7x	JTS a16 3 22/18 - - - -	OUT 24 1 12 - - - -	CTS a16 3 22/18 - - - -	OUT 25 1 12 - - - -	*JMP a16 3 22 - - - -	OUT 26 1 12 - - - -	*CAL a16 3 22 - - - -	OUT 27 1 12 - - - -	JTP a16 3 22/18 - - - -	OUT 28 1 12 - - - -	CTP a16 3 22/18 - - - -	OUT 29 1 12 - - - -	*JMP a16 3 22 - - - -	OUT 30 1 12 - - - -	*CAL a16 3 22 - - - -	OUT 31 1 12 - - - -
8x	ADA 1 10 S Z P C	ADB 1 10 S Z P C	ADC 1 10 S Z P C	ADD 1 10 S Z P C	ADE 1 10 S Z P C	ADH 1 10 S Z P C	ADL 1 10 S Z P C	ADM 1 16 S Z P C	ACA 1 10 S Z P C	ACB 1 10 S Z P C	ACC 1 10 S Z P C	ACD 1 10 S Z P C	ACE 1 10 S Z P C	ACH 1 10 S Z P C	ACL 1 10 S Z P C	ACM 1 16 S Z P C
9x	SUA 1 10 S Z P C	SUB 1 10 S Z P C	SUC 1 10 S Z P C	SUD 1 10 S Z P C	SUE 1 10 S Z P C	SUH 1 10 S Z P C	SUL 1 10 S Z P C	SUM 1 16 S Z P C	SBA 1 10 S Z P C	SBB 1 10 S Z P C	SBC 1 10 S Z P C	SBD 1 10 S Z P C	SBE 1 10 S Z P C	SBH 1 10 S Z P C	SBL 1 10 S Z P C	SBM 1 16 S Z P C
Ax	NDA 1 10 S Z P C	NDB 1 10 S Z P C	NDC 1 10 S Z P C	NDD 1 10 S Z P C	NDE 1 10 S Z P C	NDH 1 10 S Z P C	NDL 1 10 S Z P C	NDM 1 16 S Z P C	XRA 1 10 S Z P C	XRB 1 10 S Z P C	XRC 1 10 S Z P C	XRD 1 10 S Z P C	XRE 1 10 S Z P C	XRH 1 10 S Z P C	XRL 1 10 S Z P C	XRM 1 16 S Z P C
Bx	ORA 1 10 S Z P C	ORB 1 10 S Z P C	ORC 1 10 S Z P C	ORD 1 10 S Z P C	ORE 1 10 S Z P C	ORH 1 10 S Z P C	ORL 1 10 S Z P C	ORM 1 16 S Z P C	CPA 1 10 S Z P C	CPB 1 10 S Z P C	CPC 1 10 S Z P C	CPD 1 10 S Z P C	CPE 1 10 S Z P C	CPH 1 10 S Z P C	CPL 1 10 S Z P C	CPM 1 16 S Z P C
Cx	NOP 1 10 - - - -	LAB 1 10 - - - -	LAC 1 10 - - - -	LAD 1 10 - - - -	LAE 1 10 - - - -	LAH 1 10 - - - -	LAL 1 10 - - - -	LAM 1 16 - - - -	LBA 1 10 - - - -	LBB 1 10 - - - -	LBC 1 10 - - - -	LBD 1 10 - - - -	LBE 1 10 - - - -	LBH 1 10 - - - -	LBL 1 10 - - - -	LBM 1 16 - - - -
Dx	LCA 1 10 - - - -	LCB 1 10 - - - -	LCC 1 10 - - - -	LCD 1 10 - - - -	LCE 1 10 - - - -	LCH 1 10 - - - -	LCL 1 10 - - - -	LCM 1 16 - - - -	LDA 1 10 - - - -	LDB 1 10 - - - -	LDC 1 10 - - - -	LDD 1 10 - - - -	LDE 1 10 - - - -	LDH 1 10 - - - -	LDL 1 10 - - - -	LDM 1 16 - - - -
Ex	LEA 1 10 - - - -	LEB 1 10 - - - -	LEC 1 10 - - - -	LED 1 10 - - - -	LEE 1 10 - - - -	LEH 1 10 - - - -	LEL 1 10 - - - -	LEM 1 16 - - - -	LHA 1 10 - - - -	LHB 1 10 - - - -	LHC 1 10 - - - -	LHD 1 10 - - - -	LHE 1 10 - - - -	LHH 1 10 - - - -	LHL 1 10 - - - -	LHM 1 16 - - - -
Fx	LLA 1 10 - - - -	LLB 1 10 - - - -	LLC 1 10 - - - -	LLD 1 10 - - - -	LLE 1 10 - - - -	LLH 1 10 - - - -	LLL 1 10 - - - -	LLM 1 16 - - - -	LMA 1 14 - - - -	LMB 1 14 - - - -	LMC 1 14 - - - -	LMD 1 14 - - - -	LME 1 14 - - - -	LMH 1 14 - - - -	LML 1 14 - - - -	HLT 1 8 - - - -

Misc/control instructions
Jumps/calls
Load/store/move instructions
Arithmetic/logical instructions

Length in bytes → | INS reg
2 16
S Z P C | ← Instruction mnemonic
← Duration in cycles
← Flags affected

Duration of conditional calls and returns is different when action is taken or not. This is indicated by two numbers separated by "/". The higher number (on the left side of "/") means duration of instruction when action is taken, the lower number (on the right side of "/") means duration of instruction when action is not taken.
All instructions marked by "*" are only alternative opcodes for existing instructions. Those alternative opcodes should not be used.

Registers

7 0
A (accumulator)
B
C
D
E
H
L

13 0
PC (program counter)
Stack level 1
Stack level 2
Stack level 3
Stack level 4
Stack level 5
Stack level 6
Stack level 7

Flags:

S	Z	P	C

S - Sign Flag
Z - Zero Flag
P - Parity Flag
C - Carry Flag

Notes:
- Intel 8008 had internal stack 7 levels deep. In fact stack was implemented as a register file of 8 registers 14bits wide. Actual program counter was always one of them.
- There were no 16bit arithmetics nor register pairs. The only register pair was HL which was used as a memory reference and in that case was called M.
- There were two versions of 8008. 8008 with speed upto 500kHz and 8008-1 with speed upto 800kHz. In most of the manuals duration of each instruction is given in machine cycles, but each machine cycle consisted of 2 clock cycles. That's why it looks like if duration in cycles is doubled in above table. To make it clear - for 500kHz 8008 NOP took 20µs and for 800kHz 8008-1 NOP took 12.5µs.
- Unlike in 8080 there was no flag register, that's why there is no bit position given for flags.
- Address bus was 14bit wide so only 16kB of ram could have been addressed.
- 8008 had interrupt facility, but of limited use. There were no disable interrupt nor enable interrupt instructions, so interrupt was enabled all the time. As there was no instructions able to push or pop content of the register on the stack and the only memory reference was possible through HL register pair which had to be modified to store content of other registers into memory. So almost nothing could be done in interrupt service routine without changing registers which made interrupts almost unusable. A workaround was developed to overcome this problem. External hardware stack was used - content of registers could have been pushed to and popped from port connected to external stack using OUT and IN instructions.