RCA Laboratories

Research Report 1974

Princeton, N. J.

Company Private

Automated assembly equipment capable of producing 2000 assemblies per hour was installed in Somerville and became operational in October 1974. Debugging of the equipment, incorporation of design improvements, and production of test cells for reliability evaluation of the linear product are in progress. The considerable success achieved with the CA3046 is in marked contrast to the problems encountered when bonding to the COS/MOS CD4011 chips used in various logic function configurations. For reasons not clearly identified, the silicon underlying the COS/MOS CD4011 bumps spalls and lifts out when the thermocompression bond is made to the gold bump on the Ti-Pd-Au metallized interconnects. Considerable effort in analysis of this problem has not, as yet, led to any successful solution.

For further information refer to:
F. E. Scheline (Somerville).

10.4.2 Thick-Film Hybrid Technology

The choice of optimum technology for metallization of hybrid substrates has been based on either thin- or thick-film processing. A program on the use of fritless conductors in thick-film hybrid circuits was completed during 1974 and included the evaluation of characteristics, process requirements, and assembly capabilities of these conductors, as well as their compatibility with fritted thick-film resistors and dielectrics. In addition, a process for fabricating thick-film resistors terminated with thin-film metallization was developed, and the reproducibility of the fabrication process evaluated.

Elimination of the glass binder and use of reactive chemical bonding of thick-film conductor compositions has shown that, when compared with fritted conductors, fritless devices exhibit better adhesion, denser films, higher bulk conductivity, improved thermal dissipation, improved beam-lead bonding and soldering and thermocompression bonding of lead frames.

Research indicates that several advantages are obtained through the marriage of thick- and thin-film technologies. Among them are: increased resistivity ranges and power-handling capability characteristics of thin-film circuits (high megohm resistors with 100 W per square inch dissipation); improvement over normal thick-film circuit density; the achievement of thermocompression bonding of lead frames to hybrid thick/thin film circuits; and large-area, high-resolution multiple pattern processing.

The above advantages of thick/thin film technology are applicable in high-density hybrid circuits and in microwave stripline circuits.

Reference:
PRRL-74-TR-195, "Characterization of Thick Film Fritless Metallization," by R. H. Zeien.

10.4.3 Beam-Lead Chip Carriers

During the assembly of hybrid circuits utilizing beam-lead IC chips, it is essential that the chips be fully tested for both dynamic and static characteristics prior to bonding to the substrate. A carrier is under development that precisely aligns the chip beams to matching metal traces in a carrier base and establishes a reliable pressure contact between them without damage to the beams. The metal traces fan out to a configuration that permits testing when the carrier is placed into a standard socket.

The construction of the carrier permits burn-in at temperatures up to 300°C for protracted periods, repeated testing, shipment, and automatic handling and sorting without damage to the chip. Additionally, if the chip tests satisfactorily, the carrier is capable of being unloaded and the chip may be beam-lead bonded to the substrate with a minimum of manual handling.

Conceptual development was completed and prototype samples were supplied to Lockheed. Performance was satisfactory and further quantities of carriers fabricated on production tooling have been ordered. It is anticipated that by late 1975 all IC chip shipments to the Trident program will be in this type of carrier.

For further information refer to:
A. S. Rose (Somerville).

10.5 LSI Systems Design

The LSI Systems Design group has two principal objectives; to help RCA capitalize on the new technology of microprocessors, and to provide the Solid State Technology Center and Solid State Division with a resident capability in circuits, logic, and systems. In 1974 the group

successfully transferred COSMAC, a microprocessor, to SSD, as their first product in this field; the 2-chip CPU itself is now being manufactured by SSTC. Hardware prototyping kits are being manufactured by the Palm Beach Division, and several SSD customers have bought our software packages. Also in 1974, through a joint effort with SSD, our logic and systems capability was employed in the definition and implementation of a top-of-the-line multi-LSI-chip TV tuner system for Consumer Electronics.

10.5.1 COSMAC Integration

"COSMAC" is the name for a novel microprocessor architecture developed by our group in 1971 and 1972, that provides a powerful 8-bit processor capability with relatively low logic complexity. After initial breadboarding and extensive evaluation, a program was begun in 1973 to integrate COSMAC onto two COS/MOS chips, using the conventional SSD design rules and logic circuits. This was a joint program between SSTC and PBD, and in 1974 resulted in microprocessors that SSD has begun to sell and that are being installed in numerous RCA COSMAC-based systems. In 1975 efforts will be directed towards improving the yield and electrical characteristics of this product.

SOS implementations of COSMAC have also been explored. In 1974 a new approach to the layout of a one-chip processor was invented, an appropriate set of SOS logic cells developed, and certain enhancements to the architecture were defined. In 1975 the design of the one-chip SOS COS/MOS COSMAC should be completed and its evaluation begun. It's expected that this design will operate several times faster than the two-chip COSMAC.

For further information refer to:
R. O. Winder or Joel Oberman.

10.5.2 COSMAC Support

The LSI Systems Design group recognized, in 1972, the need for unusually elaborate support mechanisms for the designers of microprocessor-based systems. This support includes software development systems (assembler/simulator/debugger), hardware prototyping systems, and high-quality documentation. In 1974 a basic user's manual for the COSMAC microprocessor was prepared, which allows logic designers without computer experience to design COSMAC-based systems.

During 1974 the group's time-shared software package was converted to an easily "portable" FORTRAN-written program, providing enhancements at the same time. SSTC installed this package on NTSS and TYMSHARE. PBD installed it on the Series 70 (VMOS) system, and an SSD customer installed the package on an IBM system. Currently SSTC is installing it on the GE Timeshare Network, and is planning substantial enhancements in 1975. A manual has been written for the users of this system. It complements the basic COSMAC user's manual, and both manuals are now being sold by SSD as part of their product line, along with the chips themselves and the software package.

A COSMAC MicroKit has been designed containing a power supply, a simple control panel, and ten small printed circuit cards containing the essentials of any COSMAC-based system (clock and control memory, CPU, and simple I/O including interface to a user-supplied teletype or other terminal). The kit is packaged in a rack-mounting chassis, and provides considerable space for the user to install those additional cards required for his specific application — more memory and additional I/O controllers. Arrangements have been made with PBD to manufacture these kits; more than two dozen had been delivered to customers, mostly within the Corporation, as of mid-January 1975. A manual will be completed early in 1975.

In addition to the principal software and hardware support systems, an IBM batch-oriented assembler, a library of arithmetic subroutines and numerous I/O controllers have been developed. The assembler is being offered for sale, while the subroutines and controller designs will be provided free in the form of Application Notes.

Design was begun for an enhanced MicroKit which, provided with a "stand-alone" self assembler and an editing program, will allow engineers to design their hardware and software completely on the kit. Although less cost-effective than the use of time sharing, this approach is simpler and, initially, cheaper for the largest part of our anticipated market — engineers with no previous computer experience. SSD is expected to be selling such stand-alone systems by the middle of 1975.

A higher-level language for writing microprocessor programs will be explored in 1975.

For further information refer to:
A. D. Robbi or R. O. Winder (Somerville).

10.5.3 COSMAC Applications

FRED, the entertainment/education home computer developed in 1972, has been repackaged in LSI form. Three APAR (Automatic Placement and Routing) LSI chips were designed to work with the 2-chip COSMAC in a brief-case version of FRED. This prototype will be completed when APAR chips are received.

MicroTutor, a $300 COSMAC-based tutorial computer for learning the principles of microprocessors, has been designed and several prototypes have been built. A batch of 50 Tutors will be built in 1975 for use with a CEE video-taped course on microprocessors and for test marketing.

A prototype is being designed for a coin-operated game-playing machine. Analysis of the distribution system for this fast-growing market indicates that RCA participation is feasible. Our prototype is COSMAC-based, with FRED-type video display, and several game options stored in read-only memory (ROM). The flexibility of this approach allows the operator to change games easily (by changing ROM's), and the computer-like digital games are expected to prove very attractive to customers.

For further information refer to:
P. Baltzer or J. A. Weisbecker (Princeton).

10.5.4 Automotive Electronic Systems

In late 1973, this group was formed to complement an existing device-oriented group. The dual purpose of the new group is to conduct actual on-board testing in the harsh automobile environment and to provide a general data base for the company in this field.

One of the two vehicles the group owns has been instrumented to record such variables as temperature, pressure, fuel flow, carburetor air flow, vehicle speed, and engine vacuum. Several types of mass-flow sensors have been evaluated and recommendations for redesign have been submitted. An excellent temperature sensor has been in operation detecting engine coolant and carburetor air temperature. This vehicle is also being adapted for computer-controlled anti-skid braking experiments.

A COSMAC microprocessor kit has been adapted with proper interfaces and is operational in the test vehicle. The driver has a keyboard and a display available to him and programs have been written to record and calculate mileage, speed, miles per gallon, and fuel consumed.

Studies are proceeding to make more extensive use of the microprocessor in braking control and driver display. The latter function will encompass displaying alphanumerics and graphics to replace the existing instrument cluster. Additional warning and diagnostic information may be displayed upon driver command or by priority interrupt.

For further information refer to:
W. R. Lile, J. W. Tuska (Princeton), or A. D. Robbi (Somerville).

10.5.5 Electronic TV Tuners

Two projects were successfully completed in 1974 in the TV area — an SOS LSI chip for a frequency synthesis tuner, and a set of LSI chips as a CE product. An APAR bulk COS/MOS chip was designed for the frequency synthesis project.

The SOS chip required the design of a new library of logic cells and was also the vehicle for testing a new and efficient modular technique for the layout of LSI chips. The experiment was very successful; all logic circuits worked as anticipated, and operating chips have been fabricated. The techniques used on this project are presently being used to implement the 1-chip SOS COSMAC discussed in 10.4.1.

The LSI Systems Design group worked with CE and SSD in 1974 to define a very ambitious top-of-the-line TV tuner, which is expected to go into production in 1975. The system, consisting now of ten LSI chips, allows the remote viewer to access any channel by direct keyboard entry, and to control volume, color, and tint. It provides an elegant on-screen display of the selected channel, and generates the control voltages for varactor tuners. Our design of the overall system integrated CE ideas for display and tuner control and SSD ideas for D/A circuits and a clock function. Working with Advanced Development of CE, the group was also responsible for the detailed logic design of three of the original five chip types.

In 1975 efforts will be made to evaluate several alternative approaches to electronic tuning, most of which employ frequency synthesis. The most promising will be implemented in LSI for evaluation by CE.

For further information refer to:
G. R. Briggs (Princeton) or R. O. Winder (Somerville).

References:
N. P. Swales and J. A. Weisbecker, "COSMAC — A Microprocessor for Minimum Cost Systems," IEEE Intercon Technical Papers (1974).
J. Weisbecker, "A Practical, Low-Cost, Home/School Microprocessor System," Computer (Aug. 1974).
J. Weisbecker, "RCA COSMAC MicroTutor Manual," Oct. 1974.
J. Weisbecker, "A Simplified Microcomputer Architecture," Computer, p. 41, March 1974.

10.6 Custom Monolithics

The major objectives of the Custom Monolithics activity are to design, fabricate, test, and deliver to the equipment and system divisions of RCA complex LSI circuits utilizing the latest and most competitive technology on a quick-turn-around basis. The design of these COS/MOS, P-MOS or SOS LSI circuits might originate in the user division or in the design group of Custom Monolithics applications after many planning meetings with the user division. Dedicated pilot lines have been established to fabricate commercial as well as military prototypes, including MIL-M-38510 specifications, and low-volume manufacturing quantities of arrays. Further, Custom Monolithics personnel train and advise LSI users on potential applications while providing design assistance utilizing the most cost-effective design automation techniques.

10.6.1 Array Fabrication

The SSTC pilot line has dedicated facilities for producing custom COS/MOS, P-MOS, and SOS arrays utilizing standard documented processes. In addition, developmental processes are evaluated for future pilot line status. Such processes have included advanced SOS processing utilizing ion-implant techniques and COS/MOS (bulk-silicon and SOS) radiation-hardened processes, among others.

During 1974, the pilot line successfully processed wafers for 116 completely new artwork designs, as well as for a large number of previously designed arrays. These LSI arrays are generally larger than 200 X 200 mils in size with some arrays exceeding 300 X 300 mils. About 30,000 packaged arrays were delivered to customers in 1974. The breakdown by technology is shown for the past three years in Table 10.1. Note that the number of arrays delivered to customers has about doubled each year.

For further information refer to:
H. Borkan (Somerville).

Table 10.1 — Breakdown by Technology of LSI Arrays Processed by SSTC Pilot Line

Technology	Year	New Artwork Types Processed	Packaged Arrays Delivered
COS/MOS	1972	42	4,031
	1973	46	5,129
	1974	81	12,395
P-MOS	1972	33	2,026
	1973	40	7,677
	1974	6	13,737
SOS	1972	1	2,050
	1973	10	2,311
	1974	26	3,011
Other	1972	—	661
	1973	8	352
	1974	3	244
Totals	1972	76	8,768
	1973	104	15,469
	1974	116	29,387

10.6.2 COS/MOS on Sapphire Custom Circuits

The Solid State Technology Center evaluated the COS/MOS silicon-on-sapphire (SOS) technology to full pilot production status in July, 1974. Custom large-scale-integrated (LSI) circuits made using the self-aligned silicon-gate COS/MOS/SOS process are now available in the same manner as the bulk-silicon aluminum-gate COS/MOS and P-MOS circuits that have been available from SSTC during the last several years.

The COS/MOS/SOS process was developed at the David Sarnoff Research Center and transferred to SSTC where the reproducibility and reliability of this technology has been improved and demonstrated. The dedicated pilot line in Somerville now routinely processes 60 two-inch sapphire wafers per week. The reliability has been proven by extended life tests performed at 125°C with 10 V applied. The indicated life at 125°C is 40,000 hours MTBF (mean-time between failures) at a 60% confidence level.

The primary virtues of this SOS technology over bulk-silicon circuits are higher speed, greater density, and improved radiation hardness. Because of these characteristics, three