RCA Laboratories

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meet the needs of major military systems contractors. In 1974 processing effort will be applied toward refining the dielectric isolation technology for the achievement of lower costs and more complex array design.

The performance of integrated linear bipolar amplifiers has been limited by the need to fabricate both p-n-p and n-p-n high-performance transistors within the same circuit chip. By applying dielectric isolation and refined diffusion techniques, the successful fabrication of matched complementary bipolar transistors has been achieved. The p-n-p transistor has a beta of about 100, while the n-p-n transistor has a beta of about 200, and both devices have BV_{CEO} greater than 35 volts. The technology was applied to the design and fabrication of a beam-lead high-performance operational amplifier with a slew rate of 50 volts per microsecond, open-loop gain of 200,000, and input bias current of 175 nanoamperes. In 1974 the complementary bipolar technology will be refined to achieve maximum high-frequency performance at microwatt power dissipations.

The application of digital processing techniques to TV tuners has great potential for improving the performance and lowering the cost of commercial VHF, UHF, and cable TV systems. Key to the implementation of such a system is the ability to perform frequency division down from the gigahertz range. Computer-aided design and analysis techniques have been applied to the design of an advanced bipolar counter capable of operating over the VHF/UHF frequency bands. Bipolar processing techniques and geometries were developed to fabricate the 4-gigahertz-f_t transistors required for this design. Utilizing these design and processing techniques, samples of a fixed-ratio (divide-by-4) counter were successfully fabricated and operated up to 1300 MHz. In 1974 the counter design and technology approaches will be applied to the more complex circuits needed to implement a synthesizer approach to TV tuners.

10.5.2 Ion Implantation

Ion implantation is a technique capable of depositing precise levels of dopants in semiconductors. In 1973 the SSTC acquired its own implantation equipment. With the aid of Princeton personnel this was made operational and applied to support both engineering design and pilot production operations within the SSTC. Ion implantation is also being applied routinely to SSD COS/MOS devices to achieve tight threshold voltage control and to eliminate guard bands. Ion implantation has been successfully applied to the fabrication of integrated complementary bipolar transistors making possible the achievement of matched electrical characteristics. High breakdown voltages in excess of 25 volts in COS/MOS through the use of implanted source and drain extensions have also been demonstrated. In 1974 the SSTC implantation effort will be applied to achieving higher packing densities in COS/MOS devices. In addition, techniques for achieving the higher concentration implantation required for the practical fabrication of bipolar structures will be investigated.

10.5.3 COS/MOS Technology

Since COS/MOS is the lowest-power technology available for the fabrication of electronic systems, and the packing density can be very high, an effort has been focused on the development of the technology and design rules needed to economically increase the achievable functional complexity of these devices. Interconnections utilizing beam-lead technology provide a low-cost, reliable self-packaging method for COS/MOS chips that is extremely attractive for military and aerospace high-reliability applications.

In 1973 the COS/MOS beam-lead technology was extended to include self-aligned silicon gates. This new technology has been applied to the design of high-packing-density memories and the design and delivery of LSI devices to complete a NASA commitment. Design studies and chip layouts have also been started for a 1024-bit RAM. Aggressive design rules are employed to minimize the chip size of this 8000 MOS transistor circuit.

Read-only-memories are a significant building block in digital information-processing systems. The custom design of COS/MOS ROM's, however, is usually costly and requires significant engineering time. In conjunction with the SSTC Design Automation activity, a

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coordinated software and silicon technology development program has been completed, permitting the design, fabrication, and testing of custom ROM designs with no design-engineering involvement. Four custom 1024-bit ROM chips were supplied to the ATL activity in Camden.

A joint program was also established with Palm Beach Division for the implementation of the FRED computer with monolithic LSI techniques. The microprocessor has been partitioned in two COS/MOS chips to be fabricated in early 1974. Both chips are approximately 250 mils on a side and contain over 3000 transistors. One chip contains the ALU and control logic in a 40-pin package. The other chip contains the register matrix and associated control logic. The entire system is designed to operate over a 5-12-volt range and is compatible with T^2L levels through the use of a separate 5-volt supply line.

In 1974 the silicon-gate technology required to fabricate LSI will be refined to a higher yield process, and additional complex structures will be made in the beam-lead format. The density improvements of the new technology will be demonstrated by the fabrication of a 1024-bit RAM, a 4096-bit ROM, and the chip complement needed for the FRED computer microprocessor.

For further information refer to:
V. Alfisi, J. Oberman, W. Bosenberg, B. Baptiste, or A. Dingwall (Somerville).

10.5.4 Linear MOS Technology
A solid-state rf switch that exhibits low ON resistance (3.5 ohms) and high OFF isolation (40 dB) over the 30 to 80 MHz band has been developed for G&CS for low-power military communications applications. The technology used to fabricate this switch is based on that used to manufacture commercial VHF dual-gate MOST's. In 1974 an integrated circuit that will incorporate driving devices and circuitry along with overload protection will be developed.

COS/MOS technology was extended to the design and fabrication of a stabilized Op-Amp chip. Samples of this device are to be used in ATL programs at Camden. SSD Linear Engineering has substantial interest in marketing an RCA chopper-stabilized Op-Amp. In 1974 this design approach will be extended to the fabrication of a high-performance chopper stabilized A/D converter.

For further information refer to:
R. H. Dawson or A. G. Dingwall (Somerville).

10.5.5 Charge-Coupled Devices
The CCD technology offers unique capability for signal processing in areas of variable delay line and transversal and recursive filter application. The extremely high packing density is attractive for achieving the objective of replacing high-capacity memory drums with solid-state shift registers. During 1973 the two-phase CCD technology was transferred from Princeton to Somerville. Feasibility of both a 621-stage analog delay line and a 1000-bit memory element along with input/output and regenerate stages has been demonstrated. During 1974 efforts will concentrate on defining a pilot-line process for the Video Disc 621-stage analog delay line, development of a one-microsecond delay line for TV signal processing, and the cooperative development of a 32000-bit CCD memory chip.

For further information refer to:
R. Dawson or J. Preisig (Somerville).

10.5.6 Yield Improvement and Process Control
During 1973 in conjunction with the SSTC Design Automation Activity, a program was developed for the plotting of circuit yield and parametric information by wafer position. This will be a powerful tool for deskilling yield analysis and improvement efforts on complex devices. In 1974 this approach will be applied to the cost reduction of specific commercial COS/MOS and bipolar products for SSD.

For further information refer to:
W. Bosenberg or F. Lee (Somerville).

10.6 Integrated-Circuit Technology

10.6.1 Silicon-on-Sapphire Technology
The cost at a given performance level determines, in large measure, the market potential of an integrated-circuit technology. MOS technology has long been acknowledged as the least expensive technology, but at some sacrifice in performance. Conversely, bipolar technology has offered a higher performance at higher cost.

Figure 10.1 is a graphical display of the relative performance levels of various integrated-circuit technologies currently utilized.

An additional development of considerable significance to the utilization of these packages in production requirements is that the relatively fragile microbridges are provided with protection against shorting to the underlying circuitry. A dielectric such as SiO_2 or an organic resin capable of photoresist delineation is deposited prior to the electroformation of the bridges, and this serves as an intervening layer should the microbridge be mechanically depressed. Several thousand packages have been supplied to SSD during 1973, and extension of the technology to the application of multichip hybrid circuitry is currently in development with considerable quantities to be built in 1974.

For further information refer to:
W. J. Greig (Somerville).

10.8.3 Thick-Film Hybrid Technology

It has been shown feasible to screen and fire conventional thick-film resistors over a large (3-3/4 X 4-1/2 inch) ceramic substrate using commercially available inks, and subsequently to add thin-film conductors. The thin-film materials are standard Ti-Pd-Au layers and are used for the resistor terminations as well as for fine-line conductors. Hybrid substrates prepared with this combination of thin and thick films have been tested successfully under severe environmental exposure; they offer the advantages of laser trimming for precision resistor requirements as well as the advantages of thin-film conductor circuit density and thermocompression-bonded lead frames.

A complex multilayer thick-film substrate was designed during the year to produce a central processing unit for automotive applications. Assembly of 6 units with 10 IC chips and 360 wire bonds per unit was completed. These have been tested, repairs involving chip replacement and rebonding where necessary have been made; and these units have passed all operational requirements.

For further information refer to:
R. H. Zeien (Somerville).

10.9 LSI Systems Design

The LSI Systems Design activity has two principal objectives: to help RCA capitalize on the new technology of microprocessors and to provide the SSTC and SSD with a resident capability in systems and logic design. Towards the former goal, a specific microprocessor has been designed—COSMAC for COmplementary-Symmetry-Monolithic-Array Computer. This CPU is being integrated in bulk and SOS COS/MOS forms. Several different applications of COSMAC are being explored in various parts of the Corporation and within this group, representing more efficient engineering of old functions and new product possibilities. The group's systems capabilities are being exercised in several areas—calculator design, process control, and TV tuner systems are three examples.

10.9.1 COSMAC Integration

In 1972 COSMAC was prototyped and several experimental systems were developed. The basic architecture was found to be very well matched to a wide variety of low-cost microcomputer systems. Therefore, in 1973 two LSI integration projects were launched incorporating certain enhancements suggested by the prior experience. The first is a 2-chip bulk COS/MOS implementation, which is being carried out in the MOS Technology group with the help of the Palm Beach Division under a Technology Transfer Program. The Systems group provided the initial logic and partition and has also carried out simulation and generated test sequences. The chip sets will be fabricated in the SSTC Custom Monolithics activity and will be available in the summer of 1974.

COSMAC is also being implemented in Universal Arrays in order to permit fabrication in SOS COS/MOS. This CPU will consist of 8 chips—4 Universal Array types and 1 RAM chip (16 X 16) being designed by the Integrated Circuit Technology activity. Layouts are complete, and simulation and digitizing are in various stages of completion. Bulk COS/MOS chip sets (using standard COS/MOS RAM chips) are expected in first quarter 1974, and SOS versions soon after.

These chip sets will be used in a variety of applications, described in the following sections. In 1974 the COSMAC's will be produced in small quantities and sampled to interested customers, both within RCA and outside. Based on experience with these projects, a plan for a 1-chip version capable of factory production will be established.

For further information refer to:
J. O. Sinninger or R. O. Winder (Somerville).

10.9.2 COSMAC Support

The COSMAC microprocessor is presently being used in the following projects: the leased-channel controller of P. M. Russo and M. Lippman in Princeton; P. Baltzer's TV-"SelectaVision" project in Princeton; several data communication projects in PBD; dispersed radar signal processing in Moorestown; and the FRED projects and new projects in automotive control and process control described below. Furthermore, several SSD customers have expressed interest in using COSMAC in their systems. For these reasons, and preparing for a widening of this customer based in the summer of 1974, the basic support mechanisms established in 1972 were strengthened in 1973 and will be further strengthened in 1974.

The prospective customer for a microprocessor requires two types of support: a basic line of hardware with which he can easily build up his prototype microcomputer system, and aids in writing software. In 1973 an arrangement was made with PBD to provide prototyping hardware to the Systems group and to other customers. These systems each include a COS/MOS breadboard of the COSMAC, 4096 bytes of NMOS memory, a T^2L interface to a variety of user-chosen input/output devices, diagnostic panel, power supply, and cabinet. Several slots in the cabinet are available for control electronics that have been designed for I/O, such as audio tape cassette players, a variety of TV set displays, Execuports, the PDP11 minicomputer, a floppy disk communication lines, keyboard, and low-cost printer or magnetic strip read/write mechanism. A multiply-divide unit and a powerful TV interface have also been designed, but not yet checked out.

This hardware is appropriate for systems that require relatively sophisticated I/O controllers. A line of much simpler, smaller, and cheaper hardware is now being designed to be available during 1974.

Software support for writing programs has been provided on NTSS, the RCA Laboratories time-sharing service. It includes an editor, assembler, and interactive simulator/debugger. This system was reworked in 1973 to maintain compatibility with COSMAC architecture and to handle larger programs and more I/O devices. In anticipation of users outside RCA, the assembler language has been analyzed and slightly redefined in order to permit a simple Standard Fortran implementation—a complete Fortran support system will be available in 1974. A stand-alone software support capability is also being planned that includes a stripped-down editor and assembler and uses a second COSMAC to effect interactive debugging.

For further information refer to:
A. D. Robbi or R. O. Winder (Somerville).

10.9.3 The "FRED" System

FRED (Flexible Recreational and Educational Device) consists of a COSMAC microprocessor, 1024 bytes of semiconductor memory, simple interfaces to each of a TV and audio tape cassette player, a gravity card reader and a keyboard, and a collection of programs that demonstrate the power of this hardware in entertainment, education, and utility applications. Games, stimulants of artistic flair, simple drill-type learning programs, and calculator functions are included. In 1973 a few enhancements were made to the hardware and a few more programs were written. The main further efforts were, first, to set up a program with Random House, and secondly, to initiate FRED2, a second version of FRED, which utilizes LSI technology.

The Random House liaison is leading towards a progression of field tests of FRED (using the FRED2 hardware, which will be much cheaper than the original T^2L prototypes). The applications are now being defined in the framework of Random House individualized reading and mathematics systems, which are in widespread use in elementary schools. During 1974 the required programs will be written and this field test will be supported.

FRED2 will be built up using the 2-chip COSMAC, 3 APAR LSI chips, and about 30 standard ICP's. The required logic has been designed, breadboarded, and debugged; and it will be captured in the APAR system during 1974. First prototypes are expected in the summer. Several product divisions are following these developments and will soon be able to evaluate FRED for educational and home markets.

For further information refer to:
J. A. Weisbecker (Princeton) or A. D. Robbi (Somerville).

10.9.4 Small Business Systems

During 1973 the "Selectask" system was completed. It is based on the INTEL 8008 microprocessor, 4096 bytes of memory, a Selectric