

InterSystems Sixteen Kilobyte Static Memory

for the S-100 Bus

PRELIMINARY
SPECIFICATION SUBJECT TO CHANGE

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Ithaca InterSystems, Inc.

Manual Revision 0

Congratulations!

You have chosen one of InterSystems new Series II memory boards, the most flexible and reliable memory units for the S-100 bus.

As with all InterSystems Series II products, these memory units have been designed to take advantage of all the extensions and specifications of the new IEEE S-100 bus specification, and yet remain compatible with the majority of pre-standard S-100 boards.

This owners manual has been prepared to acquaint you with your memory unit and to serve as an aid in achieving its optimum use. In section 1 the general design and features of the unit are discussed. In section 2 specific instructions are given for the configuration of the board in your system. Section 3 contains technical reference information, and the last sections contain the parts list and schematic.

If you have any problems with the memory unit in your system, give us a call at (607) 257-0190; our technical support personnel will be glad to assist you.

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Section 1

Introduction and General Information

1.1 Features

1.2 Service Information

- Receiving Inspection
- Warranty Information
- Replacement Parts
- Factory Service
- Contacting InterSystems

1.3 Data Transfer on the S-100 Bus

- Memory Organization
- Word Transfers
- Byte Transfers

1.1 Features

The InterSystems 16 K Static RAM board is the first S-100 static memory board to take full advantage of the recent IEEE specification. Its features include:

- * Byte or Word Data Transfer. Whether you're using an 8 bit processor or one of the new 16 bit processors, the board's data bus automatically adjusts to the requested word width. You can even run a 16 bit processor and an 8 bit Direct Memory Access Controller concurrently in the same bus.
- * Standard or Extended Addressing. The memory board may be addressed in either the standard 16 bit address space (64 K), or in the extended 24 bit address space (16 megabytes).
- * High Speed Operation. The board may be configured for either 2 MHz or 4 MHz operation without wait states. All timing is completely IEEE S-100.
- * Clocked or Full Static Memory. The board has been designed to use either full static memory chips, or the new low power clocked static memory chips.
- * Phantom and Error. These new S-100 lines assist in bootstrapping and memory protection. The Phantom line is implemented as a board disable, while the Error line prevents a write to the board.
- * Low Power/Low Heat Design. Low power not only means less drain on the system power supply, but higher reliability and longer chip life as well.
- * Damped Array. All lines driving the memory array include small series damping resistors, reducing array noise and improving reliability.
- * Wait State Generator. One to three wait states may optionally be generated on the board.

1.2 Service Information

Receiving Inspection

When your InterSystems Memory Module arrives, examine the shipping container for signs of possible damage to the contents during transit. Then inspect the contents for damage. (We advise that you save the shipping container for use in returning the module to InterSystems, should it become necessary to do so).

Any apparent damage should be reported to InterSystems at once. Please write us describing the problem so that we can take appropriate action.

Warranty Information

In brief, your assembled and tested InterSystems Memory Module, and all parts supplied, are warranted against defects in materials and workmanship for a period of 1 year from the date of purchase. Refer to Appendix I for the complete Statement of Warranty.

Replacement Parts

If you find a bad component on your Memory Module, a memory chip for example, return it to us with a letter. We will replace it and return it with a "no charge" invoice if the unit is under warranty. Out-of-warranty parts prices may be confirmed by telephone.

Factory Service

InterSystems provides a factory repair service for all of its products. Before returning the module to InterSystems, first obtain a Return Authorization Number from our Technical Service Dept. This may be done by calling us, sending us a TWX, or by writing to us. After the return has been authorized, proceed as follows:

- 1) Write a letter describing the problem
- 2) Describe your system to us, list boards by Manufacturer and name.

- 3) Include Xerox copies of the schematics of boards by manufactures other than InterSystems.
- 4) Include the Return Authorization Number.
- 5) Pack the above information in a container suitable to the method of shipment.
- 6) Ship prepaid to InterSystems.

Your module will be repaired as soon as possible after receipt and return shipped to you prepaid.

Contacting InterSystems:

The following apply both for correspondence and service.

Ithaca InterSystems Inc.
1650 Hanshaw Rd.
P.O. Box 91
Ithaca N.Y. U.S.A.
14850

Telephone (607) 257-0190
TWX 510 255-4346

In Europe:

Ithaca InterSystems Ltd.
58 Crouch Hall Rd
London N8 8HG. U.K.

Telephone 01-341-2447
Telex 299568

1.3 Data Transfer on the S-100 Bus

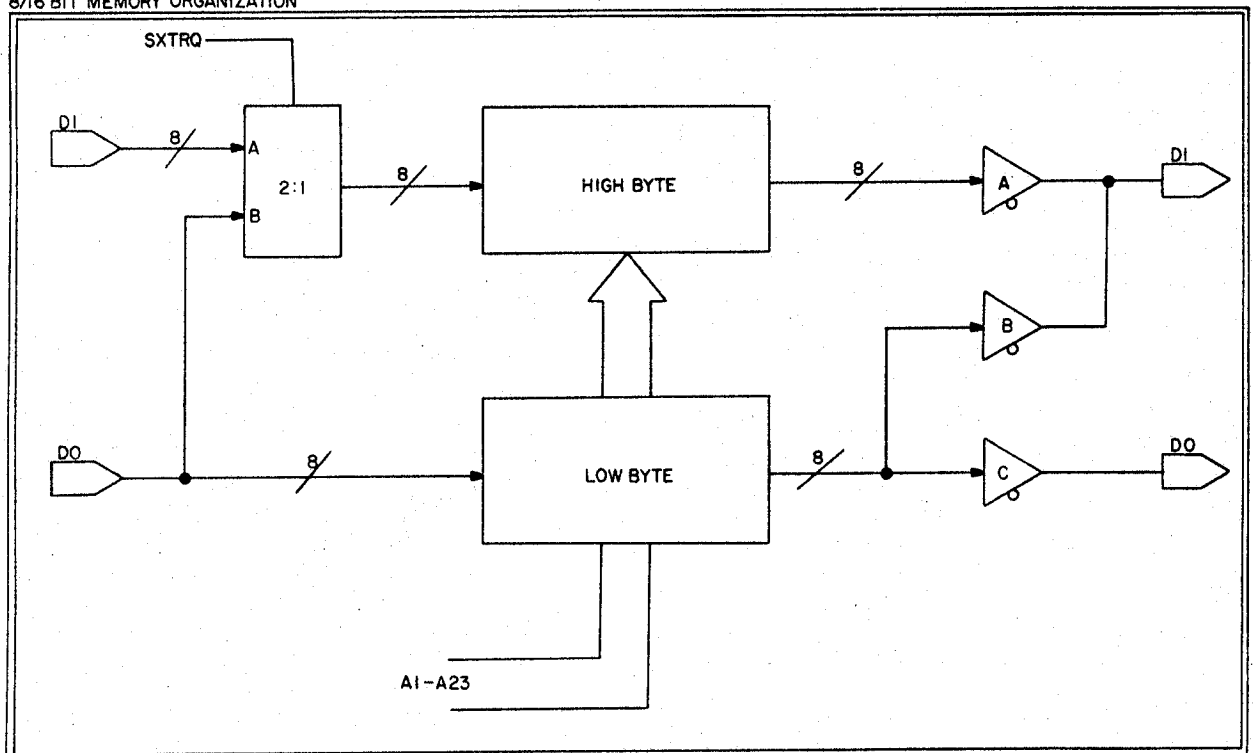
The S-100 data bus supports both byte parallel (8 bit) and word parallel (16 bit) data transfers, hence allowing both 8-bit and 16-bit processors to use the same memory boards, or even to co-exist in a single system. For 8-bit data transfers the 16 data lines are grouped into two uni-directional 8-bit busses, the Data In Bus and the Data Out Bus. For 16 bit data transfers, the two uni-directional busses are ganged to form a single 16-bit bi-directional data path.

An additional status line has been assigned to control the grouping of the data lines, called Sixteen Request (sSXTRQ). This line is asserted when the processor requests a 16-bit data transfer on the bus. 8 bit processors do not generate this line, and hence the data transfer proceeds in byte mode.

Memory Organization

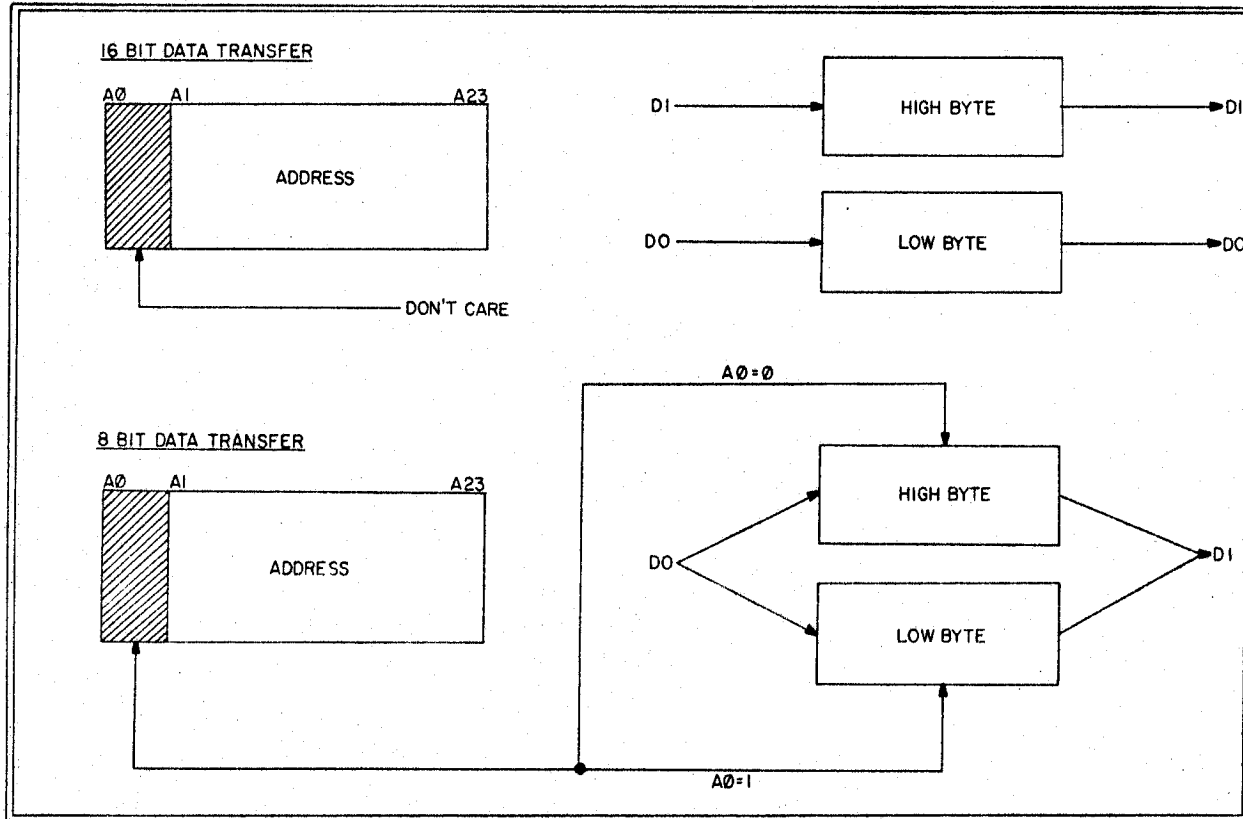
To be capable of both 8-bit and 16-bit parallel transfers memory is organized as two banks of 8-bit memory, one bank for the most-significant-byte of the 16-bit word, and one bank for the least-significant-byte. These banks may be activated either together or separately, depending on the condition of the sixteen request status line. This basic memory organization is shown in figure 1.

FIGURE 1
8/16 BIT MEMORY ORGANIZATION



Memory in S-100 systems is always addressed as bytes. And since a word is composed of two bytes, the least significant address bit, A0, is not considered in address decoding for word (16 bit) references. For byte references however, the A0 bit selects either the most significant byte or the least significant byte within the addressed word. See figure 2.

FIGURE 2
8/16 BIT ADDRESS AND DATA USAGE

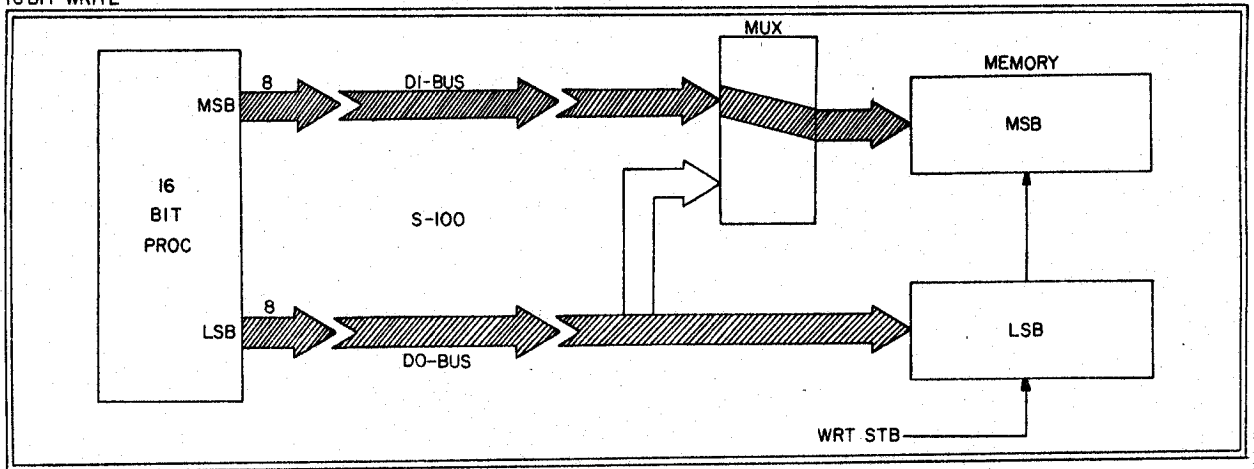


Word Transfers

For word, or 16-bit, data transfers the processor asserts the word memory address on address lines A1-A23 (A15 for short address systems), and the Sixteen Request line.

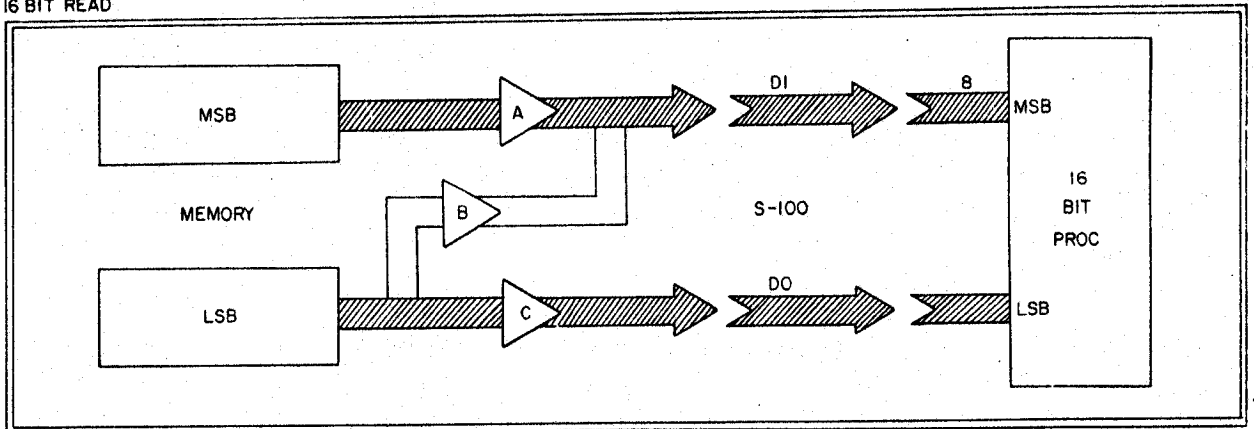
During a write operation, data is output from the processor on the 16 data lines. The least significant data byte is routed to the data lines of the least-significant memory bank via the D0 lines. The 2 to 1 multiplexer on the data input lines of the most significant bank is selected such that the most significant data byte, asserted by the processor on the DI lines, is routed to the data input lines of the most significant bank. The write strobe from the processor writes the data into both banks simultaneously. See figure 3.

FIGURE 3
16 BIT WRITE



The 16-bit read operation follows a converse path. Data to be input to the processor is routed from the memory array banks to buffers A and C (figure 4) and then to the data lines on the bus during the read strobe. Again the data from the most significant byte is routed via the DI bus, and data from the least significant byte via the DO bus.

FIGURE 4
16 BIT READ



Byte Transfers

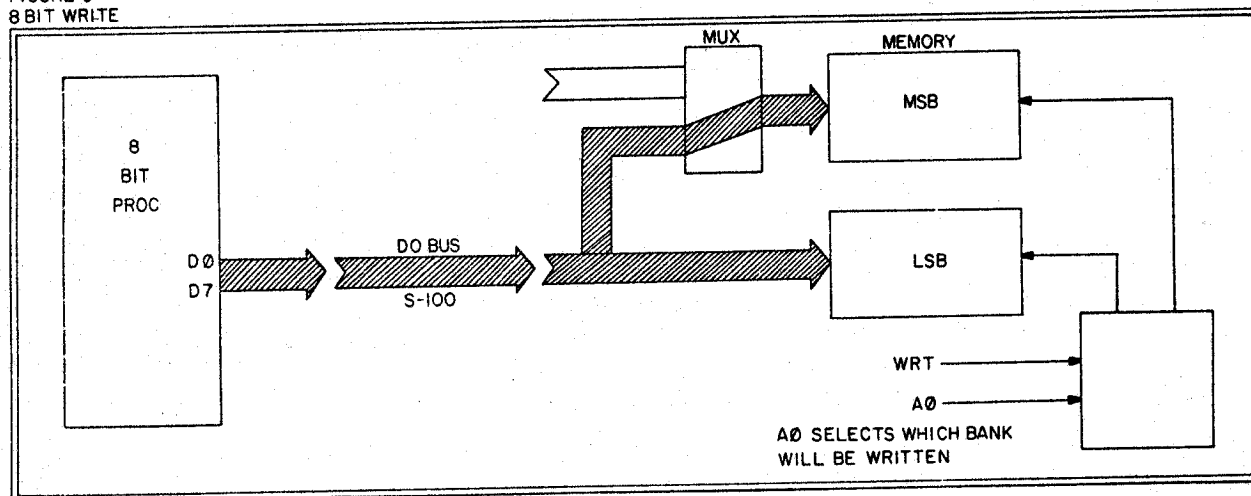
If the Sixteen Request line is not asserted, the memory reference is conducted as a single byte transfer. The processor asserts the memory word address on address lines A1-A23, and selects the proper byte within the word by asserting the A0 line.

According to the IEEE specification, if A0 is False (electrically low) the most significant byte within an addressed word is selected; if A0 is true,

the least significant byte is selected.

Figure 5 shows the data path for an 8 bit write operation. Data is asserted by the processor on the Data Out Bus, where it is connected to the data input lines of both memory banks; the data input lines of the least significant bank are connected directly to the D0 lines, and the data input lines of the most significant bank are connected to the D0 lines through the 1 to 1 multiplexor controlled by the Sixteen Request line.

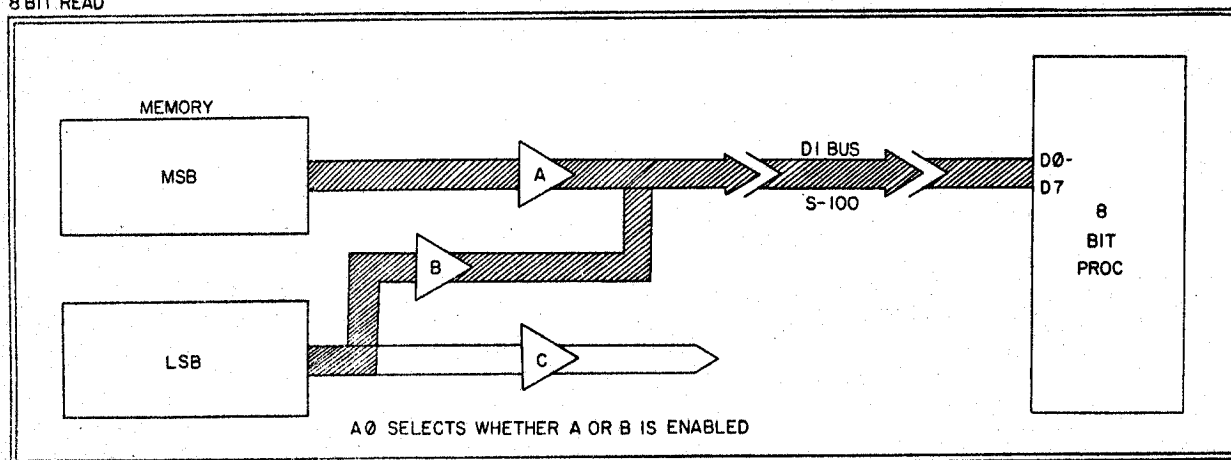
FIGURE 5
8 BIT WRITE



The write strobe asserted by the processor is gated with the A0 line so that only the correct byte is written within the selected word.

The 8 bit read operation is illustrated in figure 6. The 16 bits of data from the memory array goes to buffers A and B. Only one of these buffers will be enabled, depending on the condition of the A0 line. The selected buffer gates the correct byte onto the Data In Bus, where it is received by the processor.

FIGURE 6
8 BIT READ



Section 2

Board Setup and Installation

2.1 Standard and Extended Addressing

2.2 Wait State Generation

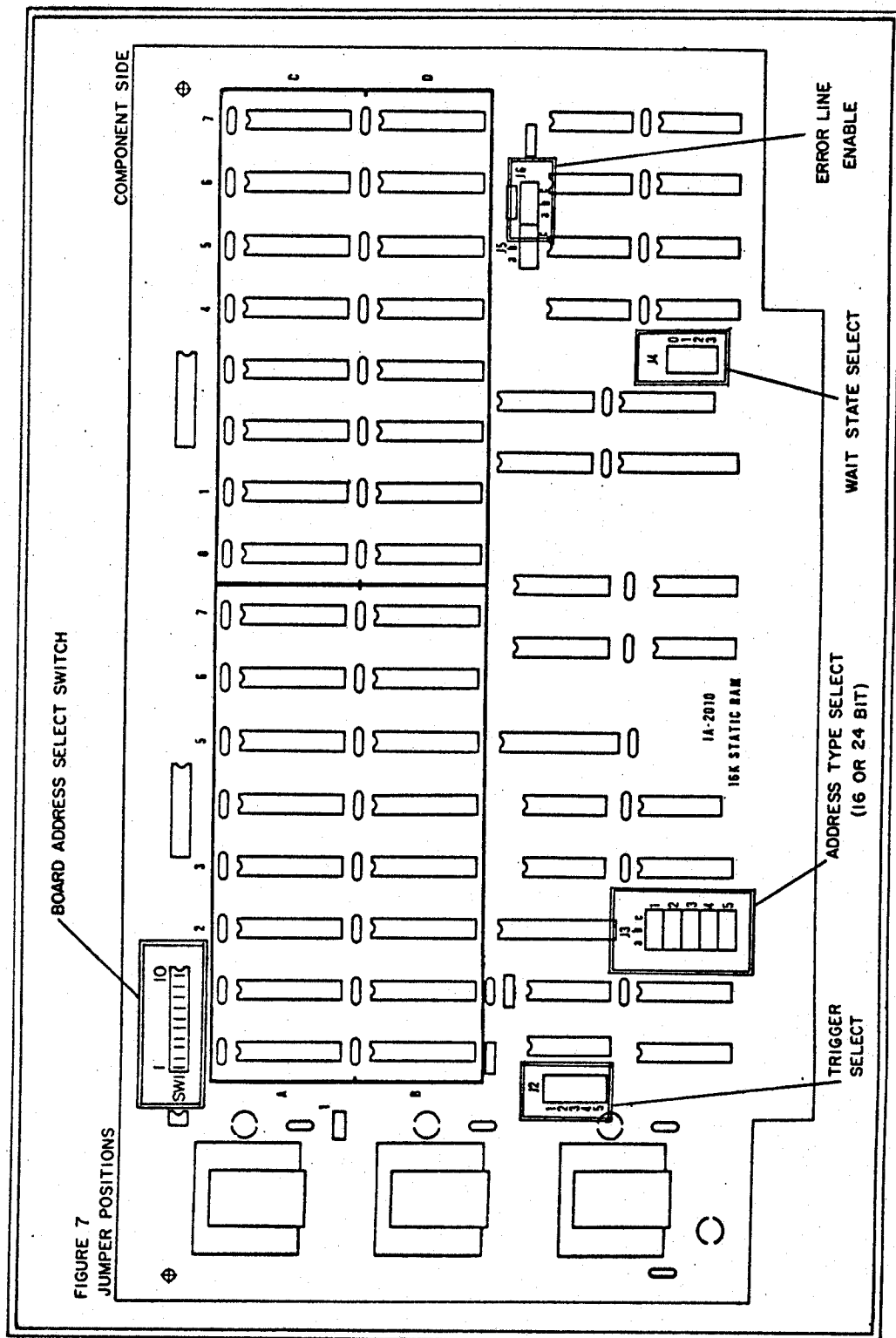
2.3 Board Triggering

2.4 Error Line Implementation

2.5 Jumper Summary

2.6 Installing the Board

2.7 Bad Chip location



2.0 Board Setup

This section of the manual describes how to set the memory board up for operation in your system. Certain jumpers on your board are only used in assembly or in testing, and these will be described only in the technical reference section.

This section describes the base address selection of the board in either 16 bit or 24 bit address space, wait state selection, and optimum board triggering for different S-100 processors.

Figure 7 shows the board location of the jumpers we are concerned with in this section.

2.1 Standard and Extended Addressing

The IEEE S-100 bus has two addressing modes. Standard addressing provides a memory address space of 64 kilobytes while the extended address mode provides memory addressing to 16 megabytes.

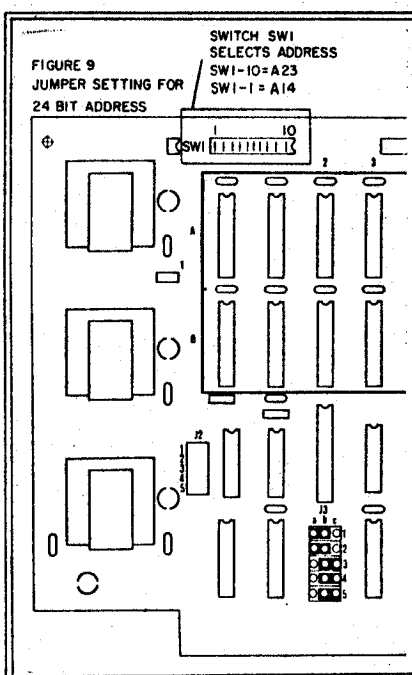
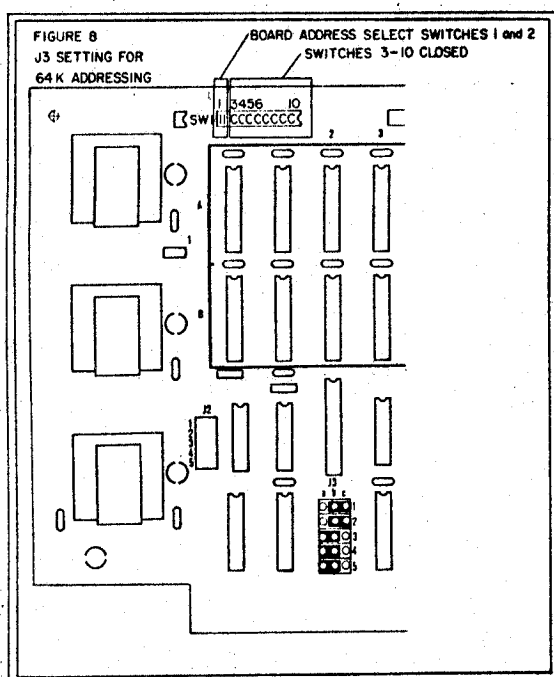
The Sixteen K board may be addressed in either of these modes, using jumper J3 and the DIP switch SW1.

Standard Addressing (16 bit)

To configure the board for a 16 bit address space, jumpers in area J3 should be configured as follows:

J3-1 = B to C
J3-2 = B to C
J3-3 = A to B
J3-4 = A to B
J3-5 = A to B

And switch positions 3, 4, and 5 of switch SW1 should be closed. See figure 8.



The board may now be addressed at any 16 K boundary within a 64 K address space. The location is selected with switches 1 and 2 of SW1. Switches 6 through 10 of SW1 do not enter into the decoding in standard addressing mode, and may be in either position.

64 K Addressing

0-15 K	SW1-1 = C	SW1-2 = C
16-31 K	SW1-1 = 0	SW1-2 = C
32-47 K	SW1-1 = C	SW1-2 = 0
48-63 K	SW1-1 = 0	SW1-2 = 0

Where C = Closed or On and 0 = Open or Off.

Extended Addressing (24 bit)

To use the extended address mode of the board the J3 jumpers should be configured as follows:

J3-1 = A to B
J3-2 = A to B
J3-3 = B to C
J3-4 = B to C
J3-5 = B to C

The address of the memory board within the 16 megabyte range may now be selected with the switches at SW1. Figure 9 shows the configuration of jumpers for 24 bit addressing.

The 64 K page in which the memory appears is selected using switches SW1-3 through SW1-10, where SW1-3 corresponds to address bit A16 and SW1-10 corresponds to A23. These switches define the matching address which selects the board. An open switch will match an address bit which is logically high, while a closed switch matches a logically low address bit.

For example, if we wish to address the board in page 00, then all the switches in positions 3 through 10 should be closed and the switches in positions 1 and 2 select which 16 K block within the 00 page the board will respond to.

Another example:

Address the board in page 4B(hex) in the first 16 K block.

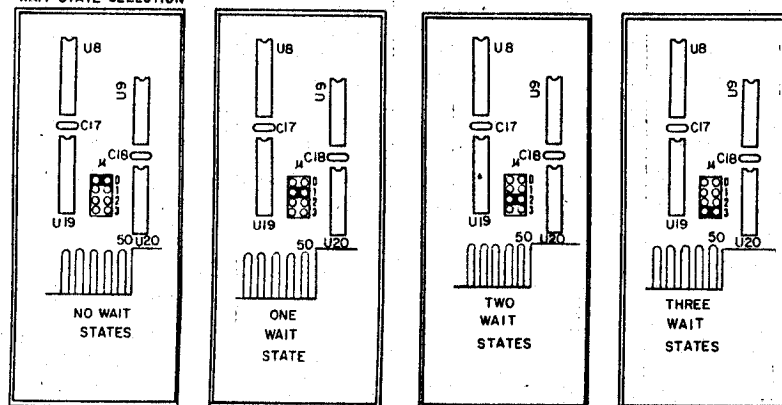
Address	4	B	0
Binary	0100	1011	00
Switch Setting	COCC	OC00	CC
Switch Pos.	(10).....1		

Note that in both these configurations the PHANTOM line on the bus acts as a board disable line, that is, the board may neither be written to nor read from if the PHANTOM LINE is asserted on the bus.

2.2 Wait State Generation

The Sixteen K board has an on-board wait state generator that generates zero to three wait states according to the jumper setting in area J4. See figure 10.

FIGURE 10
WAIT STATE SELECTION



2.3 Board Triggering

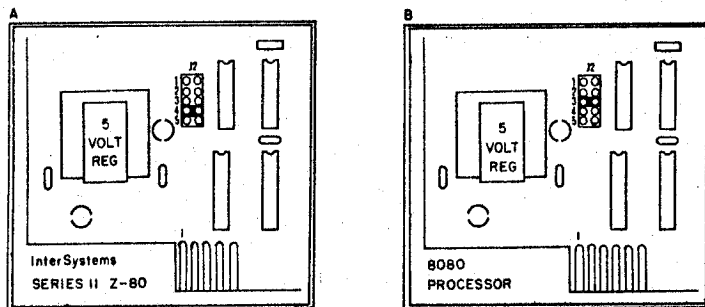
In order to achieve the most reliable operation of your memory board, it is necessary to determine the best moment in your processor's bus cycle to trigger the memory board. This board triggering is controlled by jumper J2, in the lower left corner of the board.

The following list of popular processors for the S-100 bus should serve as a guide to setting the jumper; if your processor is not included, position 3 is most likely to work, position 4 is second choice. Note that 4 Mhz. Z-80 processors by manufacturers other than Ithaca Audio / InterSystems may require a wait state added to the Instruction Fetch cycle (M1).

Manufacturer	Board	Speed	J2 Setting
InterSystems	Series II Z-80	2/4	4
InterSystems	Series II Z-8000	2/4	1
Ithaca Audio	Z-80	2	3
Ithaca Audio	Z-80	4	2
(all)	8080	2	3

Figure 11a shows an example setting of jumper J2 for the InterSystems Series II Z-80 board, figure 11b shows the setting for all 8080 processors.

FIGURE 11
BOARD TRIGGERING (J2)



Note: On the North Star Z-80 board, the status line SW0 is not true until very late in the bus cycle for memory write operations. Hence, this board will require modification to the processor board before correct triggering will be achieved.

2.4 Error Line Implementation

The IEEE S-100 bus has a generalized error indication line called ERROR. This line may be used in a number of ways; parity error, write to protected memory, etc.

The InterSystems 16 K board implements this line as a write protect line, so that memory management for an entire S-100 system may be implemented in a central location.

However, unless you are using such a system, the ERROR line jumper, J5, should be connected in the inactive position.

Error line (J5)

Active	A to B
Inactive	B to C

2.5 Jumper Summary

This is a summary of the jumper settings described in this section. For complete information refer to the sub-section concerned with a specific jumper.

Address Bus 16 Bit Address:

J3-1, J3-2	BC
J3-3, J3-4, J3-5	AB
SW1-3 THRU SW1-10	CLOSED
SW1-1, SW1-2	Base Address Select

SW1-1	SW1-2	BASE ADDRESS
C	C	0000 (HEX)
O	C	4000 = 16K
C	O	8000 = 32K
O	O	C000 = 48K

24 Bit:

J3-1, J3-2	AB
J3-3, J3-4, J3-5	BC

SW1-3 Thru SW1-10 PAGE SELECT (which 64K page)

SW1-3 Matches A16
SW1-10 Matches A23

A closed switch matches a TRUE address bit (electrically high).

SW1-1, SW1-2 BASE ADDRESS SELECT(as above)

Wait States:

J4-0	=	0	WAIT STATE(S)
J4-1	=	1	" "
J4-2	=	2	" "
J4-3	=	3	" "

Board Triggering:

Manufacturer	Board	Speed	J2 Setting
InterSystems	Series II Z-80	2/4	4
InterSystems	Series II Z-8000	2/4	1
Ithaca Audio	Z-80	2	3
Ithaca Audio	Z-80	4	2
(all)	8080	2	3

Error Line:

J5	AB	=	ENABLED
J5	BC	=	DISABLED

2.6 Installing the Board

Once you have selected the board address, trigger point, and set the wait state generator, you can now install the board in your system.

With the system power off, insert the board into the S-100 bus, taking care not to skew the card fingers with respect to the edge connector (it is possible with some card edge connector sockets to skew the board such that the gold fingers on the board seat between the brushes of the socket).

Turn on the system power and run a memory test program such as TSTMEM, which is supplied with all InterSystems Disk Operating Systems, over the address space covered by the new memory board.

Your memory board has been extensively tested and burned in at high temperatures before shipment from the InterSystems plant, and should work the first time. If you do have trouble however, here are some pointers:

Power down the system. Check the following:

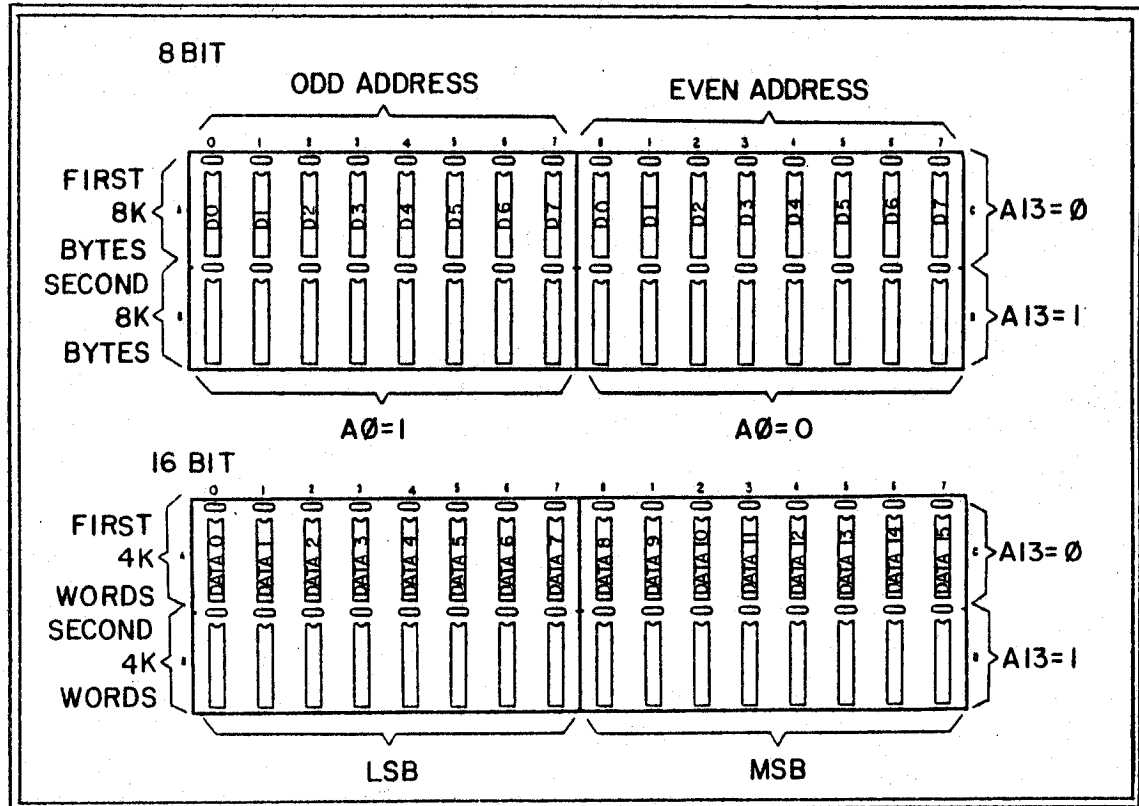
- 1) Is the board seated in the edge connector properly?
- 2) Has one of the chips on the board been jarred loose in shipping?
- 3) Is the Trigger set properly? If your CPU was not listed above, and you guessed at this, try another position.
- 4) Try adding a wait state. Is the board you ordered the right speed for your system? If the Trigger is set too late, the board may appear to need a wait state.
- 5) How's your power supply? Check the +8 volt line on the bus (pins 1 and 51). If it's less than 6.5 volts, this could be the problem.
- 6) Is one of your old boards generating bus line 58? This line, now the IEEE line indicating a 16 bit data transfer request, may have been assigned a special function by a manufacturer of pre-IEEE S-100 boards.

If none of the above solve your problem, or if you need any assistance whatsoever, give us a call at (607) 257-0190.

2.7 Bad Chip Location

If you have a single bad memory chip on your board, as indicated by your memory test program, this section will help you locate the bad chip on the memory board. Memory Chip location is summarized in figure 12.

FIGURE 12
BAD CHIP LOCATION



For both 8 bit and 16 bit systems the first 8 K bytes of memory (addresses < 2000 Hex) are located in areas A and C, while the second 8 K bytes (addresses = or > 2000 Hex) are located in areas B and D.

8 Bit Systems

In 8 bit systems bytes with even addresses are located in areas labeled C and D, while bytes with odd addresses are located in areas A and B.

Within each lettered area are 8 memory chips. The chip labeled 0 corresponds to data bit 0, the chip labeled 7 corresponds to data bit 7.

An example:

A memory error is indicated at location 03A6(hex) in Data Bit 5. The memory board is addressed in the first 16 K of memory. Address 03A6 is (1) in the first 8 K of memory (2000 H is the first location in the second 8 K), and (2) the address is even. From figure 12 we see that the bad chip is located in area C. The chip labeled 5 (data bit 5) in area C is the bad chip.

Sixteen Bit Systems

In sixteen bit systems the data bits 0 through 7 are located in memory chip areas A and B and data bit numbering corresponds to chip numbering. The data bits 8 through 15 are in areas C and D, with the chip numbered 0 corresponding to data bit 8 and the chip numbered 7 corresponding to data bit 15.

Section 3.0

Technical Reference Section

3.1 Memory organization

24 Bit Address Decoding
16 Bit Address Decoding

3.3 Board Select Signal

3.4 Data Input Circuit

3.5 Data Output Circuit

3.6 Wait State Generator

3.7 Write Strobe Generation

3.8 Chip Enable Circuit

3.9 Timing Diagram

3.0 Technical Reference

This section describes the operation and organization of the circuits of the InterSystems Sixteen K board. It is intended for maintenance personnel rather than for the general user and contains no user information not elsewhere contained in the manual.

3.1 Memory Organization

Memory on the Sixteen K board is organized as 2 pages of 4K by 16 bit words, with address line A 13 selecting between the pages. Page 0 (A 13=0) consists of memories in areas A and C, Page 1 (A 13=1) of memories in areas B and D. Within a particular memory area the chip labeled 0 corresponds to the least significant bit within that byte, and the chip labeled 7 corresponds to the most significant bit. Area A and B contain the least significant bytes within 16 bit words, and C and D contain the most significant bytes. This is indicated in figure 12. A 16 bit word within a page is selected by bus addresses A1 through A 12.

For word operations (16 bit parallel) the A0 bit does not enter into the decoding, but is assumed to be a logical 0. All 16 bit words in S-100 memory start on even address boundaries.

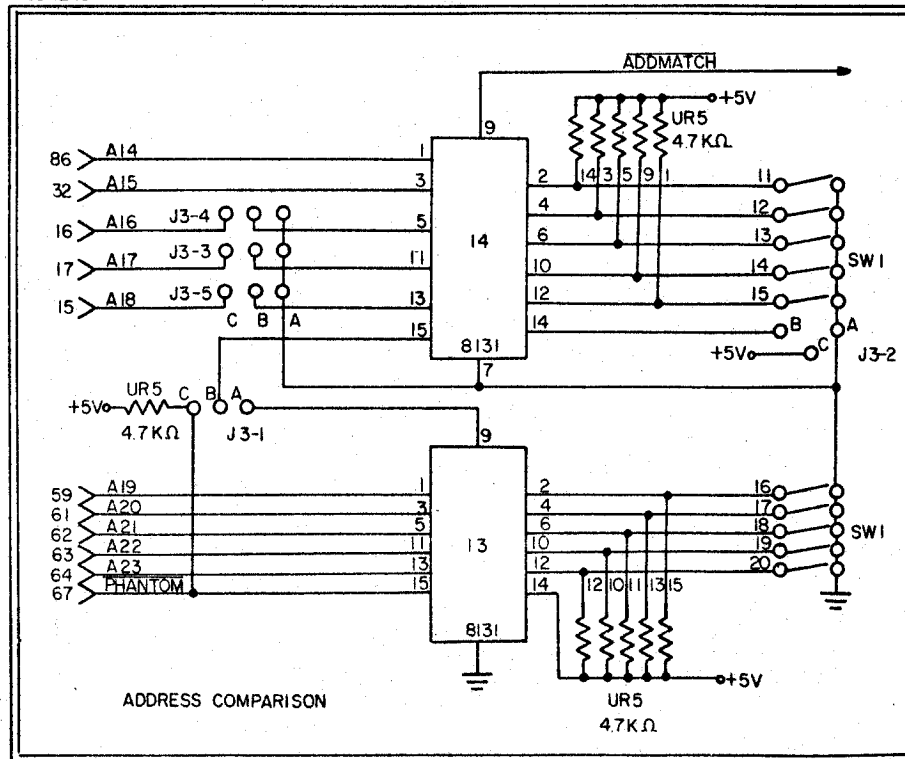
For 8 bit operations the A0 address bit selects the most significant byte or the least significant byte within the addressed word by, in the case of a read operation, conditioning the read strobe (DBIN), or, in the case of a write operation, by conditioning the write strobe (MWRT) such that only a single byte of the addressed word is operated upon.

A0 = 0 Selects Most Significant Byte
A0 = 1 Selects Least Significant Byte

3.2 Address Decoding

The board will decode either a 16 bit (64 Kilobyte) address space or an extended 24 bit address space (16 Megabyte). In either case the PHANTOM line is decoded as a board disable line. This is according to the IEEE bus, and represents a change from some traditional usage of the Phantom line as a read disable. Figure 13 gives a partial schematic of the address decoding circuit.

FIGURE 13



24 Bit Address Decoding

24 Bit Address Decoding is conducted by two cascaded 8131 6 bit comparators, U13 and U14, operating in unlatched mode. These compare the bus address bits A 14 through A 23 and the condition of the Phantom line with the user selectable board address from the switches at SW1.

In the 24 bit mode the jumpers at J3 should be configured such that J3-1 cascades the two comparators (A to B), J3-2 matches the correct output polarity of the first comparator (A to B), and J3-3,4, and 5 are connected to address lines A 16, A 17, and A 18.

16 Bit Address Decoding

In the 16 bit address mode the high address comparator is strapped out of the circuit; its' output is replaced by the Phantom line as cascade input to the low order comparator. This is done by connecting J3-1 between B and C and changing the polarity of the matching bit (J3-3, B to C). The Address bits A 16, A 17, and A 18 are jumpered out of the circuit by connecting J3-3, 4, and 5 between A and B. Switch positions SW1-3, 4, and 5 must be closed in the 16 bit mode to match the disconnected address lines.

Two address lines receive special consideration by the control circuitry, A0 and A 13. The A 13 line selects between banks of 16 bit words, and the

A0 line selects between bytes of an addressed word during byte operations.

All other address lines drive the memory array through inverting bus receivers and 27 ohm series damping resistors. The series damping resistors serve two functions. The first is to reduce the reflections within the memory array, thereby reducing array noise and crosstalk, and the second is to current limit the AC load on the array drivers during address changes.

3.3 Board Select Signal (BDSEL)

The board select signal is an on board status signal which combines the output of the address comparison circuit with the current cycle status information on the S-100 status bus. The logic equation of this signal, generated at U20 pin 13 is:

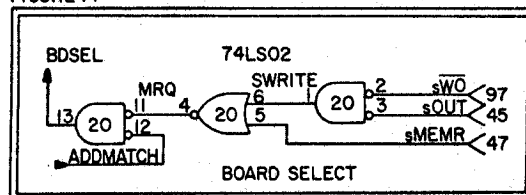
$$\text{BDSEL} = \text{/ADDMATCH} * (\text{sMEMR} + (\text{/SWO} * \text{/SOUT}))$$

WHERE: * is logical AND
+ is logical OR
/ is logical NOT

and ADDMATCH and SWO are active low signals.

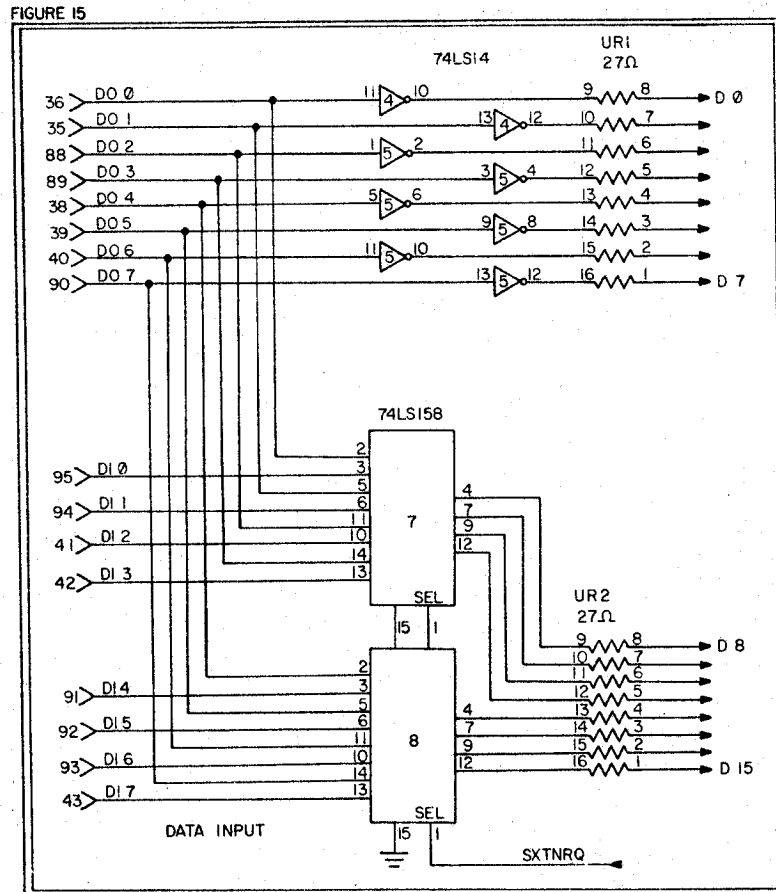
This equation, roughly translated, means that the board is selected if the address on the bus matches the board address and the status on the bus indicates either a memory read or a memory write operation. A schematic of this circuit is given in figure 14.

FIGURE 14



3.4 Data Input Circuit

The data input circuit consists of a set of bus receivers and a 2 to 1 multiplexor. Figure 15 gives the data input schematic.



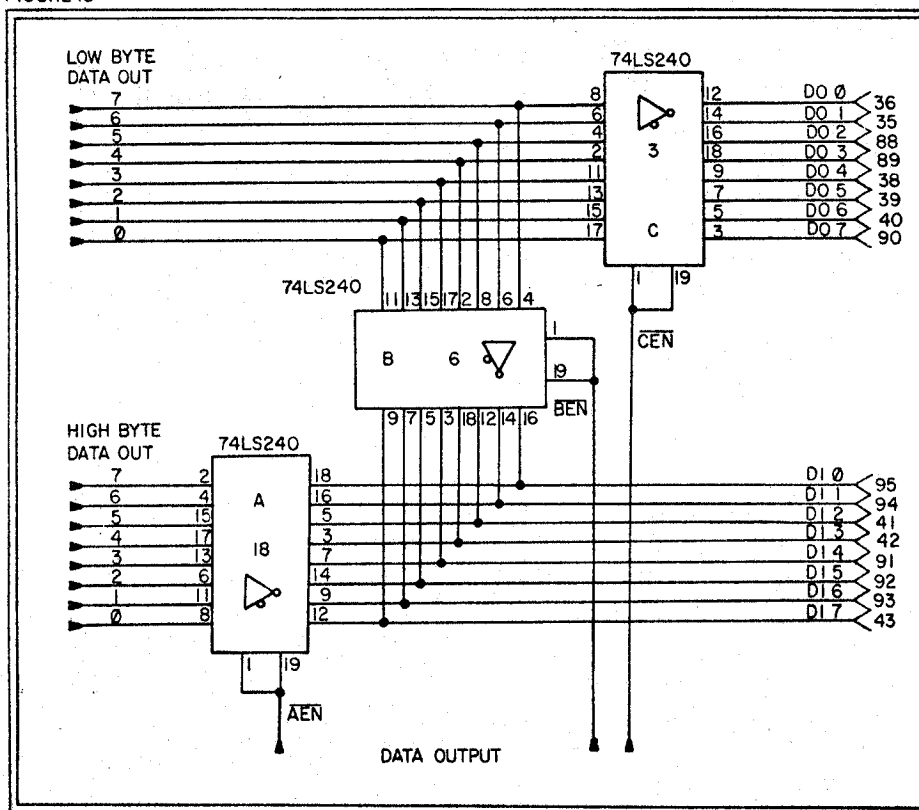
For an 8 bit operation the data input lines from both the most significant byte and the least significant byte are driven by the 8 data lines of the S-100 Data Out (D0) bus. The data input lines of the LSB are driven through bus receivers U4 and U5 and series damping resistors. The data input lines of the MSB are driven through 27 ohm damping resistors by 2 to 1 multiplexors, U7 and U8, which select inputs according to the condition of the Sixteen Request line. In the 8 bit case, the 8 lines from the D0 bus are routed to the data input lines of the most significant byte.

For 16 bit operations on the other hand, the Sixteen Request line switches the multiplexor to the other inputs, the DI bus, driving the memory array with 16 bits of parallel data rather than duplicate bytes.

3.5 Data Output Circuit

The data output circuit consists of three octal 3-state drivers, U3, U6, and U18, represented by the buffers A, B, and C in figure 16.

FIGURE 16



For 16 bit read operations the 16 bit output data from the memory array is gated onto the S-100 16 bit data path by the read strobe, DBIN, through buffers U3 and U18. For 8 bit read operations however, only one of U6 or U18 is turned on with the read strobe, depending on the condition of the A0 line, thus gating only the requested byte onto the Data Input (DI) bus. The logic equations which control the enabling of these buffers are as follows:

$$\begin{aligned} \text{U3-ENABLE} &= \text{SXTRD} \\ \text{U6-ENABLE} &= \text{EGHTRD} * /A0 \\ \text{U18-ENABLE} &= (\text{SXTRD}) + (\text{EGHTRD} * A0) \end{aligned}$$

WHERE:

$$\begin{aligned} \text{SXTRD} &= \text{BDSEL} * /\text{SXTRQ} * \text{DBIN} \\ \text{EGHTRD} &= \text{BDSEL} * \text{SXTRQ} * \text{DBIN} \end{aligned}$$

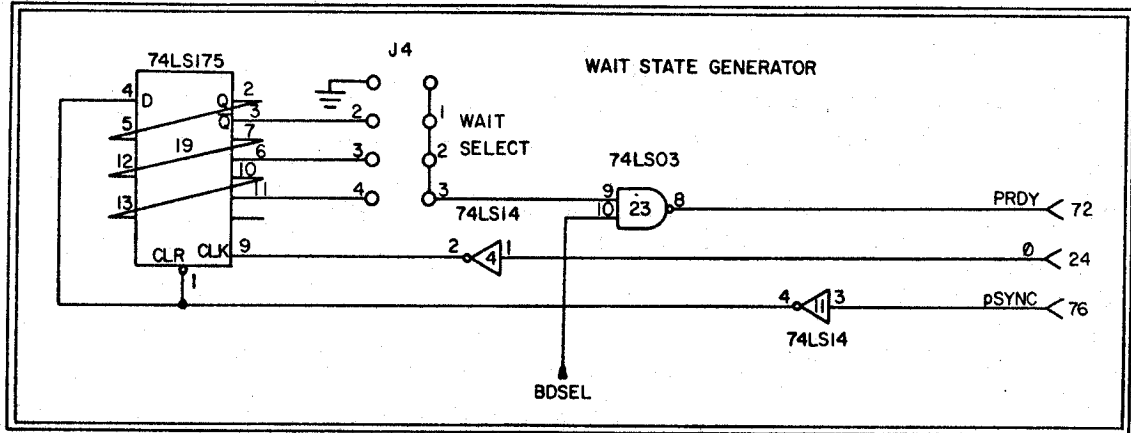
Note: SXTRQ is an active low bus signal.

3.6 Wait State Generator

Optional wait states may be generated by a three stage Johnson counter, U19.

The counter is cleared by the PSYNC pulse, and begins its countdown on the first falling edge of the system clock ϕ (phi) after the PSYNC interval. If the board has been selected for the current cycle, a wait state lasting 0 to 3 clock cycles will be asserted on the Ready line through an open collector driver. The length of the wait request depends on which tap of the counter has been selected at J4. Figure 17 shows the wait state generator.

FIGURE 17



3.7 Write Strobe Generation

The write strobes for the MSB and the LSB banks are generated separately for byte operations and simultaneously for word operations. For byte operations the write strobes are conditioned by the state of the A0 line such that only the correct byte within the addressed word is written. The logic equations for the write strobes LWR (low write, U15 pin 13) and HWR (high write, U15 pin 4) are:

$$\begin{aligned} \text{LWR} &= \text{SXTWR} + (8\text{WR} * \text{A0}) \\ \text{HWR} &= \text{SXTWR} + (8\text{WR} * \text{A0}) \end{aligned}$$

WHERE:

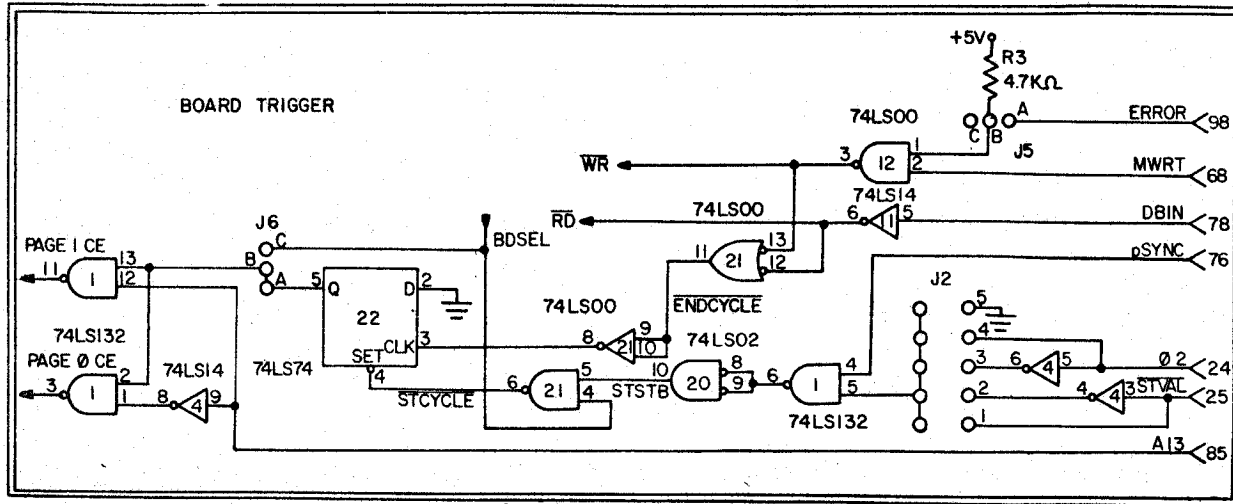
$$\begin{aligned} \text{SXTWR} &= \text{BDSEL} * \text{SXTRQ} * \text{MWRT} \\ 8\text{WR} &= \text{BDSEL} * \text{SXTRQ} * \text{MWRT} \end{aligned}$$

Note: SXTRQ is an active low bus signal.

3.8 Chip Enable Circuit

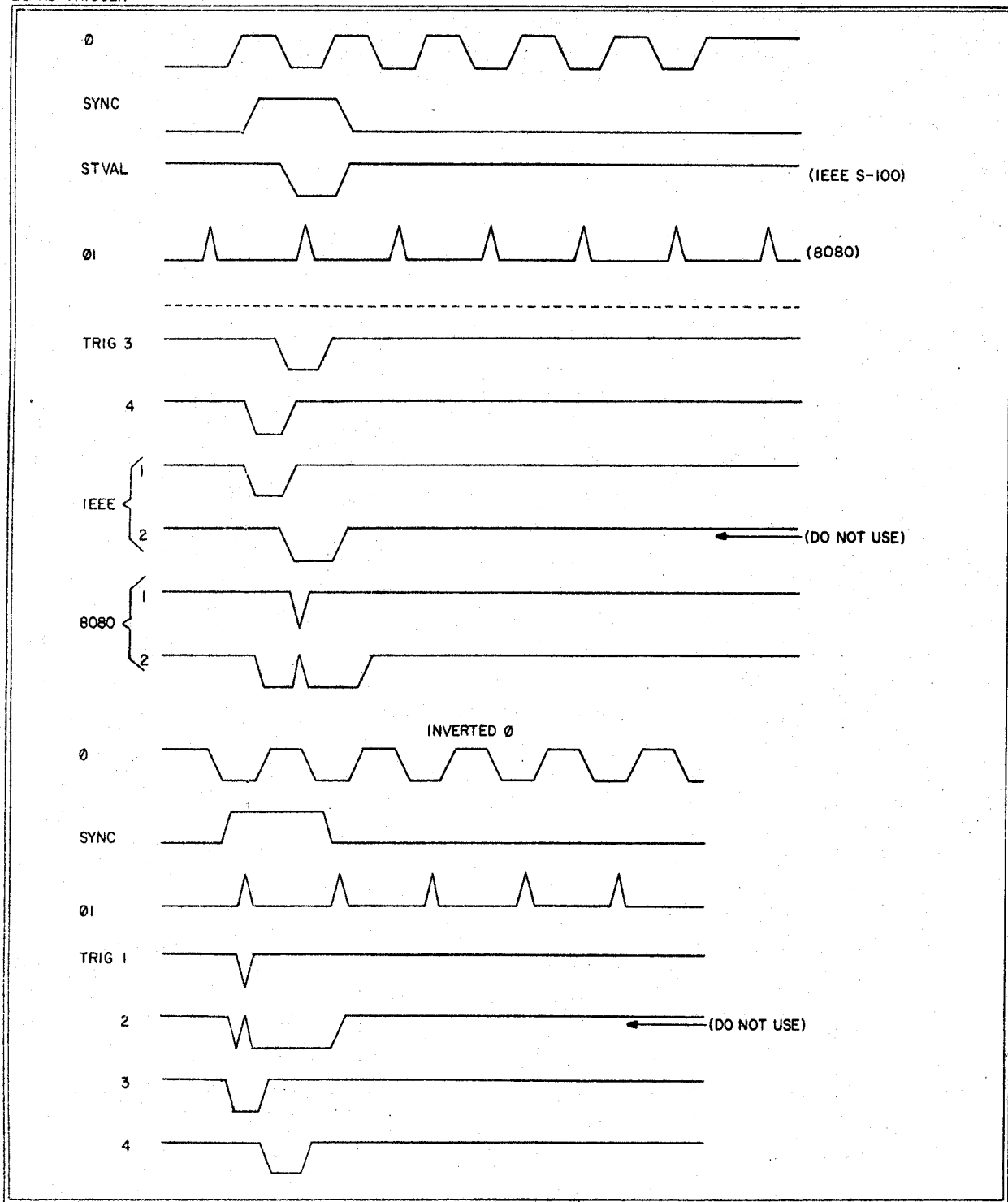
The chip enable circuit has been designed such that both full static memory chips (ex: TMS 4044) or low power edge activated chips (ex: Zilog 6104) may be used in the memory array. This is done by generating a set pulse for the chip enable flip-flop at the earliest moment in the PSYNC interval when address information has been valid for a minimum setup time.

FIGURE 18



Since there have been many implementations of bus cycle timing on the pre-standard S-100 bus, J2 has been provided to select optimum start cycle triggering for the board. Figure 19 shows the different start cycle pulses for different settings of the jumper. The falling (trailing) edge of either the MWRT strobe or the DBIN strobe provides an end cycle clock that clears the chip enable flip-flop. The output of the flip-flop is gated with the A13 signal, to generate the chip enable for either banks A and C (A13 = 0) or banks B and D (A13 = 1).

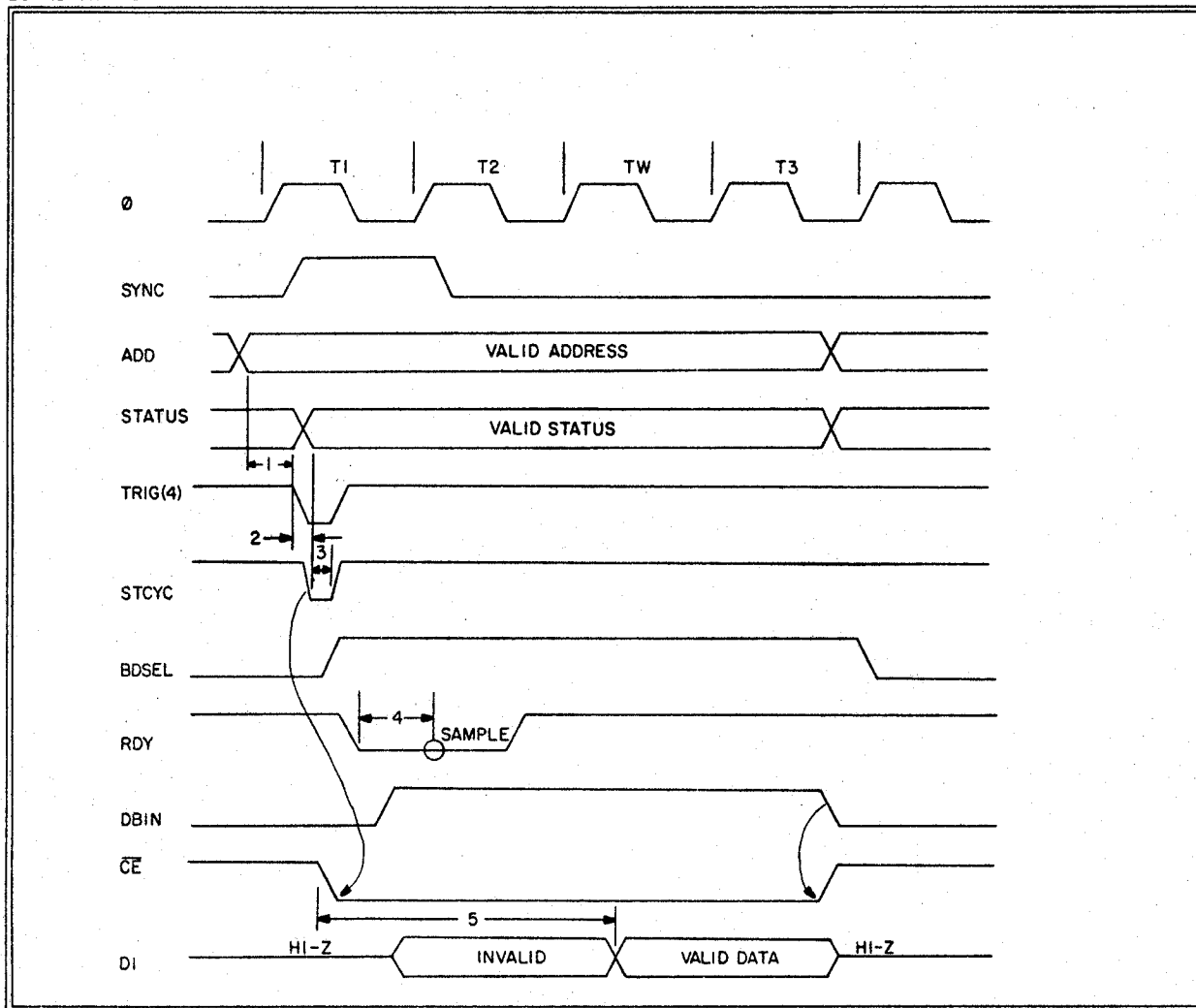
FIGURE 19
BOARD TRIGGER



3.9 Timing Diagram

Figure 20 illustrates the board timing when used with an InterSystems Series II Z-80 board. One wait state has been added to illustrate the operation of the circuit, but is not necessary for the correct operation of the two boards.

FIGURE 20
BOARD TIMING



Section 4

Parts List and Parts Placement Diagram

4.0 Parts List and Placement

Figure 21 gives the parts placement on the circuit board.

16 K Parts List

Memory Chips:

32 of Zilog Z-6104 or TI TMS-4044

Logic:

U1	74 LS 132	U12	74 LS 00
U2	(SPARE)	U13	8131
U3	74 LS 240	U14	8131
U4	74 LS 14	U15	74 LS 02
U5	74 LS 14	U16	74 LS 04
U6	74 LS 240	U17	74 LS 04
U7	74 LS 158	U18	74 LS 240
U8	74 LS 158	U19	74 LS 175
U9	74 LS 32	U20	74 LS 02
U10	74 LS 27	U21	74 LS 00
U11	74 LS 14	U22	74 LS 74

Resistors:

UR1-4	27 OHM RESISTORS, 8 SEPARATE IN 16 DIP
UR5	1 KOHM RESISTORS, 15 RES. PIN 16 COMMON
R1	27 OHM, 5%
R2	27 OHM, 5%
R3	1 KOHM, 10%
R4	1 KOHM, 10%

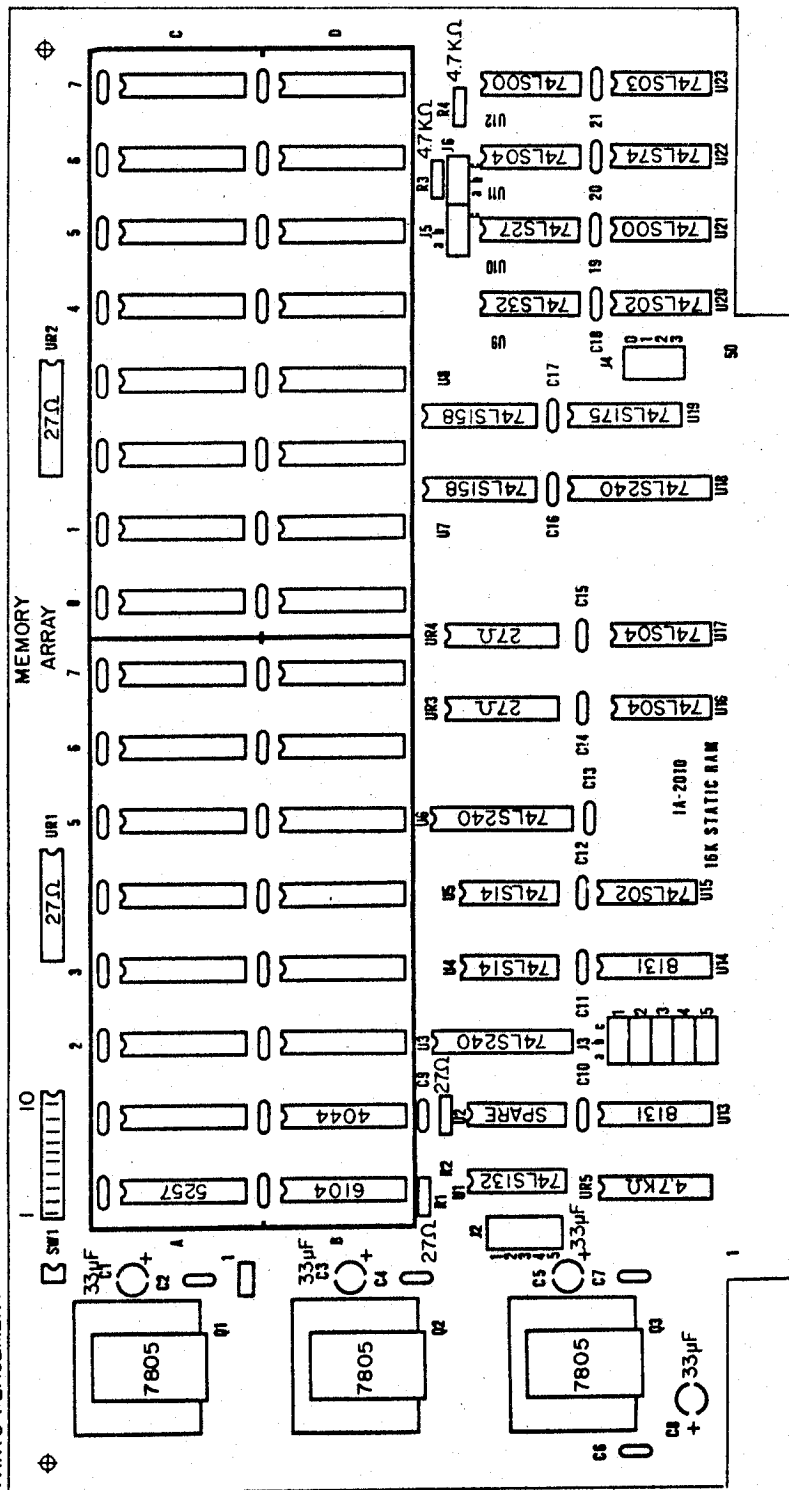
Capacitors:

C3,C6,C9	33 UFD DIPPED TANTALUM, 20 VOLTS
(all others)	.1 UFD 15 VOLTS, .3 INCH SPACING

Other:

Q1,Q2,Q3	7805, +5 volt regulator.
SW1	10 position DIP switch.

FIGURE 21
PARTS PLACEMENT



Section 5

Appendixes

- I Statement of Warranty
- II A0 Polarity
- III Memory Chip Data Sheets

Appendix I - Intersystems Warranty

Appendix II - A0 Polarity

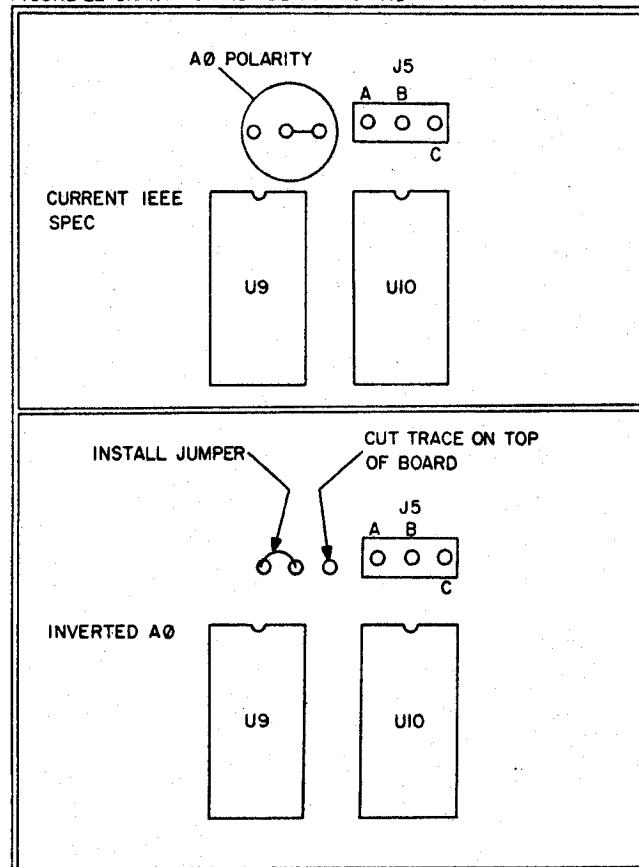
The current IEEE specification concerning which polarity of the A0 line selects which byte within an addressed word may change in the near future, and hence an unlabeled jumper has been included on the board which will change the polarity of the A0 line. This jumper, located directly to the left of J5, has a trace on the top side of the PC board between the center tap and the left tap. This configuration corresponds to the most recent publication of the IEEE committee (Computer:Jul 79) such that:

A0 = 0 Selects Most Significant Byte
A0 = 1 Selects Least Significant Byte

Should this specification change, cutting the small trace between the center and left pads, and connecting the center and rightmost pads will invert the polarity of the A0 line. Figure 22 illustrates the change.

Note that this specification is important only in systems which mix 8 bit and 16 bit transfers, in dedicated 8 bit systems, it makes no difference.

FIGURE 22 CHANGING THE POLARITY OF A0



Z6104

4096 x 1 Bit Static RAM

Product Specification

JANUARY 1978

Preliminary

- 4096 X 1 organization
- Static data storage circuitry (no refresh required)
- Single phase chip enable clock generator circuitry
- Separate data in and data output pins
- Access/Cycle times:

Access/Cycle times:	Operating power*	
100/160 ns	320 mW	Z6104-1
150/240 ns	320 mW	Z6104-2
200/320 ns	320 mW	Z6104-3
250/380 ns	165 mW	Z6104-4
300/440 ns	165 mW	Z6104-5
350/510 ns	165 mW	Z6104-6

*T_A = 70°C

- All input pins are TTL voltage level compatible
- Single +5V power supply (±10%)
- Industry standard 18 pin DIP
- Advanced depletion load N channel silicon gate technology

The Zilog Z6104 is a 4096 x 1 static RAM, fabricated using n-channel depletion load silicon gate technology. Polysilicon load resistors are used in the 64 x 64 memory array, resulting in a very small die size.

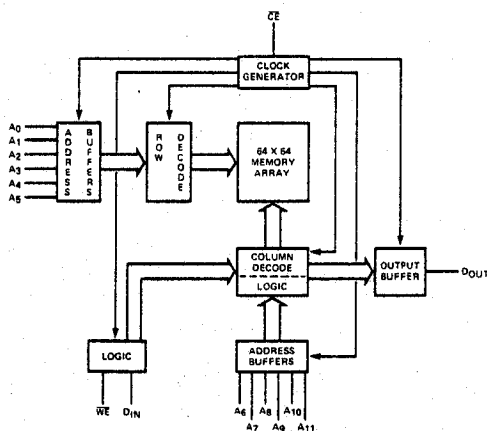
CHIP ENABLE is used as the clock input to the RAM. The HIGH-to-LOW edge of CE initiates data movement within the chip, resulting in the appearance of valid data at the DOUT pin. When CE is HIGH, the device is in the precharge mode and the chip's standby power is reduced from its operating power. Since the Z6104 is static, CE can be stopped at any time in the precharge mode without the loss of data.

The twelve address pins select a cell within the memory array. These inputs are strobed into the RAM address buffers with the CE HIGH-to-LOW edge.

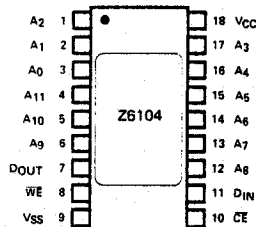
WRITE ENABLE controls the circuit's read/write function. When the RAM is activated by CE, a LOW voltage on WE writes the data presented at the DIN pin to the selected memory cell.

Virtually all MOS circuits draw less current at elevated temperature than at cold temperature. For this reason, the Z6104 has two power limits. The cold limit is necessary for system power supply design while the hot limit is useful for thermal air movement calculations.

DOUT is capable of driving two TTL loads or up to eight low-power Schottky TTL loads to standard TTL voltage output levels. All inputs are specified to standard TTL input voltage limits.



Pin Connections

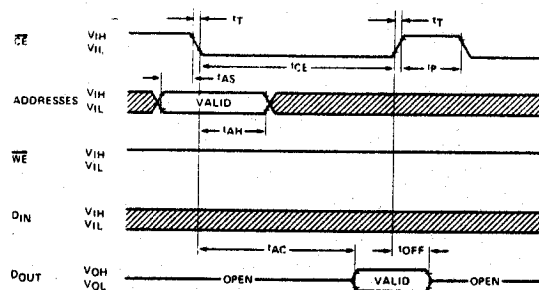


Pin Names

A0 - A11	ADDRESS INPUTS
CE	CHIP ENABLE
DIN	DATA INPUT
DOUT	DATA OUTPUT
VSS	GROUND
VCC	POWER (+5V)
WE	WRITE ENABLE

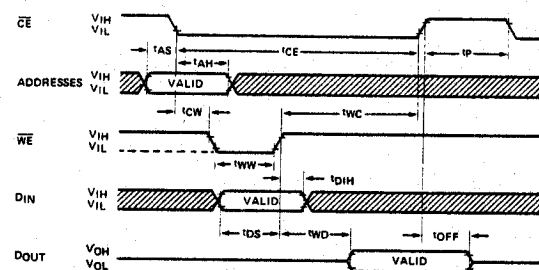
The twelve address pins have their information latched on \overline{CE} 's low going edge.

With \overline{WE} HIGH, \overline{CE} 's HIGH-to-LOW transition will cause the information stored at the location specified by the address inputs to appear at D_{OUT} . D_{OUT} starts in the high impedance mode (inactive) and goes to a low impedance mode (active) after the access time. When \overline{CE} returns HIGH, D_{OUT} goes inactive.

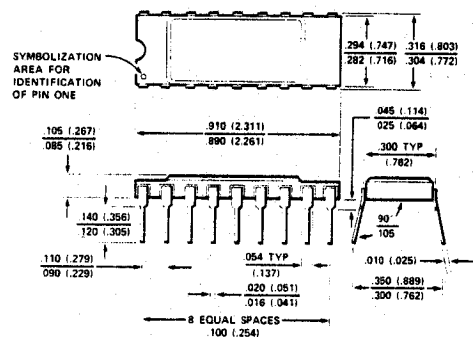
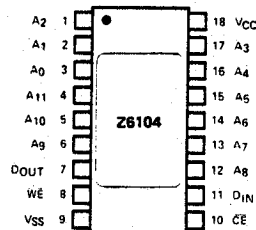
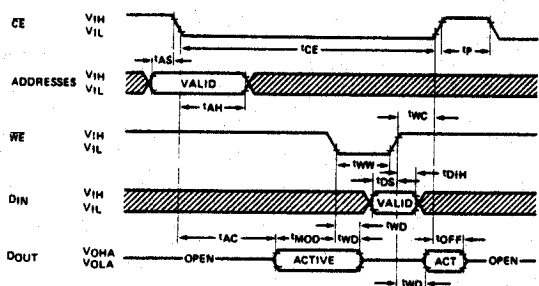


Data to be written into the chip from the Data Input pin is loaded into the selected location on the later occurring edge of \overline{CE} or \overline{WE} . The data must remain stable for the required set-up and hold times about either \overline{WE} or \overline{CE} edge, whichever occurs first. When writing, D_{OUT} is inactive, but when \overline{WE} returns HIGH, D_{OUT} goes active indicating the logic state of the addressed cell until \overline{CE} returns HIGH.

It is possible to use the 6104 in an "early write" mode. \overline{WE} can be taken LOW at or before the beginning of the cycle, but \overline{WE} cannot go HIGH until $(t_{CW} + t_{WW})$ after \overline{CE} 's LOW-going edge.



This is an extension of the Read and Write cycles. Data is read after an access time and in the same cycle is modified with a Write operation. For this cycle D_{OUT} starts inactive, and goes active after the write. At the end of the cycle, signified by \overline{CE} 's positive edge, D_{OUT} becomes inactive.



NOTE: Dimensions in parentheses are for metric system (cm).

Voltage on any pin relative to V_{SS} -0.3V to +7.0V
Storage Temperature (Ambient) -65°C to +150°C
Power Dissipation 1.5 Watts
Temperature under bias Specified operating range

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

(0°C < T_A < +70°C)

SYMBOL	PARAMETER	Z6104		UNIT
		MIN	MAX	
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IH}	Logic 1 Voltage (All Inputs)	2.0	V_{CC}	V
V_{IL}	Logic 0 Voltage (All Inputs)	-0.3	0.8	V

(0°C < T_A < +70°C) ($V_{CC} = 5.0V \pm 10\%$)

10°C < T _A < +70°C (V _{CC} = 5.0V ± 10%)		T _A = 0°C				T _A = 70°C				UNIT
SYMBOL	PARAMETER	Z6104-1,2,3		Z6104-4,5,6		Z6104-1,2,3		Z6104-4,5,6		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I _{CC1}	Average V _{CC} Power Supply Current (1)		80		40		58		30	mA
I _{CC2}	Standby V _{CC} Power Supply Current (2)		60		30		44		23	mA
I _{I(L)}	Input Leakage Current (any input)		10		10		10		10	μA
I _{O(L)}	Output Leakage Current (2, 3)	-10	10	-10	10	-10	10	-10	10	μA
V _{OH}	Output Logic 1 Voltage (I _{OUT} = -200 μA)	2.4		2.4		2.4		2.4		V
V _{OL}	Output Logic 0 Voltage (I _{OUT} = 3.2 mA)		0.4		0.4		0.4		0.4	V

- NOTES: 1. A function of \overline{CE} duty cycle. Measured with duty cycle of $t_{CE}/(t_{CE} + t_p)$
2. $\overline{CE} @ V_{IH}$
3. $0.4V \leq V_{OUT} \leq 5.5V$

(0°C < T_A < +70°C) ($V_{CC} = +5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{IC}	Input Capacitance ($\overline{CE}, \overline{WE}$)		5	pF
C_I	Input Capacitance ($A_0 - A_{11}, D_{IN}$)		5	pF
C_O	Output Capacitance		10	pF

(0°C < T_A < + 70°C) (V_{CC} = +5.0V ± 10%)

SYMBOL	PARAMETER	Z6104-1		Z6104-2		Z6104-3		Z6104-4		Z6104-5		Z6104-6		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _C	Read or Write Cycle Time (3)	160		240		320		380		440		510		ns
t _{AC}	Random Access (1)		100		150		200		250		300		350	ns
t _{CE}	Chip Enable Pulse Width	100		150		200		250		300		350		ns
t _p	Chip Enable Precharge Time	40		60		80		100		120		140		ns
t _{AH}	Address Hold Time	40		50		80		100		120		140		ns
t _{AS}	Address Set-up Time	0		0		0		0		0		0		ns
t _{OFF}	Output Buffer Turn-off Delay (2)		40		40		50		60		80		100	ns
t _{CW}	Chip Enable to Write Enable	40		50		60		80		100		120		ns
t _{DIH}	Data Input Hold Time	30		40		40		40		40		40		ns
t _{WW}	Write Enable Pulse Width	40		40		50		60		80		100		ns
t _{MOD}	Modify Time		100		100		100		100		100		100	μs
t _{WD}	Write Enable to Data Out (2)	0	40	0	50	0	60	0	80	0	100	0	120	ns
t _{DS}	Data Input Set-up Time	50		60		70		80		100		120		ns
t _{WC}	Write Enable to Chip Enable	0		0		0		0		0		0		ns
t _T	Transition Time		50		50		50		50		50		50	ns

- NOTES: 1. Output loaded with 100pF and 2 TTL loads. Output levels are V_{OH} = 2.0V and V_{OL} = 0.8V
2. Output waveform is dependent on output load. D_{OUT} is guaranteed to be OFF within t_{OFF}.
3. t_C = t_{CE} + t_p + 2 · t_T

C – Ceramic

P – Plastic

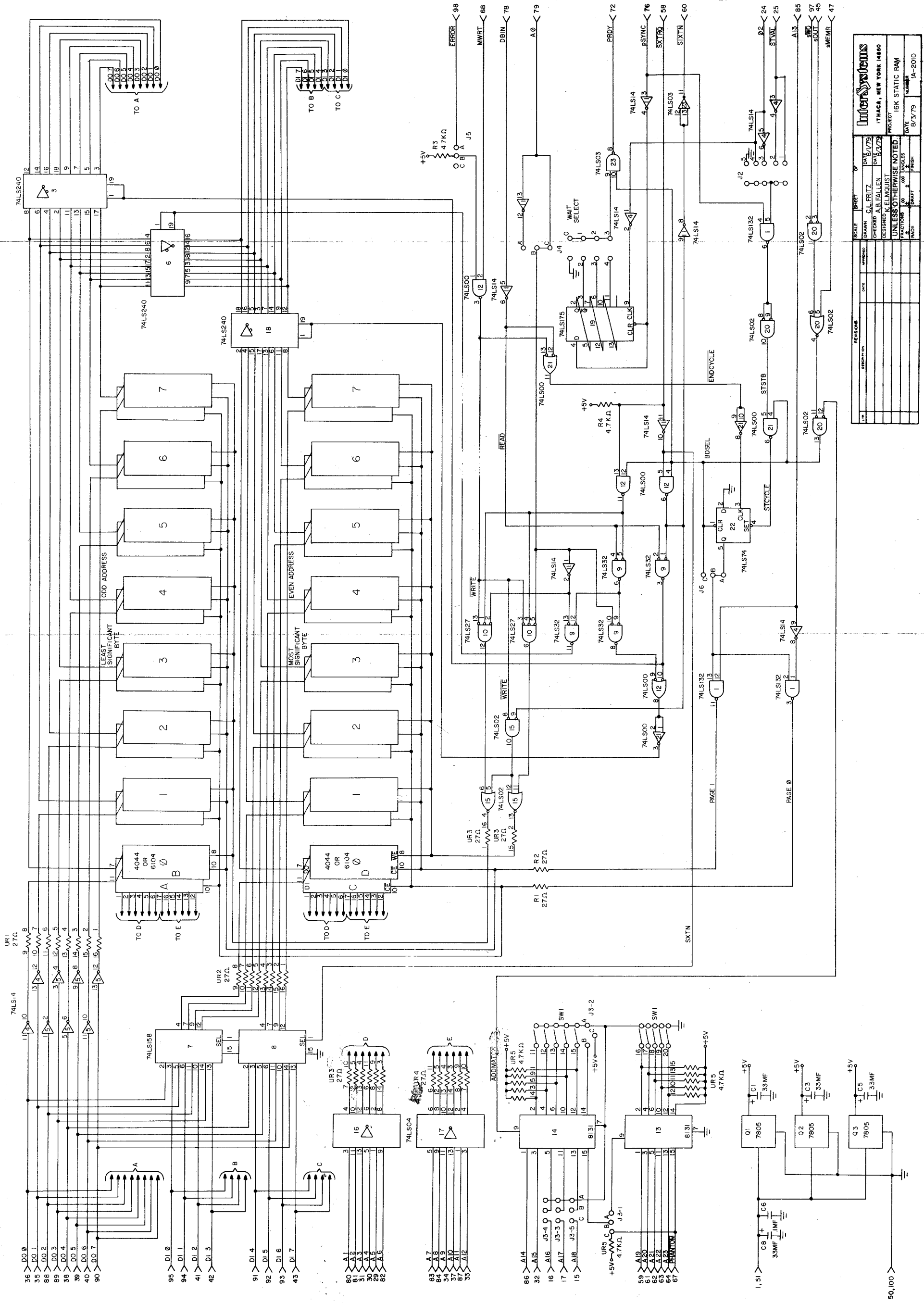
S – Standard 5V ±10% 0°C to 70°C

Example:

Z6104CS (Ceramic – Standard range)

Section 6

Schematic Diagram



InterSystems	
SCALE	SHEET
DATE	DATE
DESIGNED	DATE
CHECKED	DATE
PROJECT	PROJECT
UNLESS OTHERWISE NOTED	UNLESS OTHERWISE NOTED
REVISIONS	REVISIONS
DATE	DATE
BY	BY
DESCRIPTION	DESCRIPTION
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
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ITHACA INTERSYSTEMS IA2010 16K Static RAM

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